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SUMMARY

A 32-channel CMOS multiplexer was tested at room temperature and at liquid-helium temperature (4.9 K). Voltage gain of the FET input stage, leakage current, electrical crosstalk, and noise as a function of clock frequency were measured. The voltage gain measured at 4.9 K was slightly higher than that measured at 300 K and was independent of clock frequency at both operating temperatures. The off-channel leakage current was 0.23 pA/channel at 4.9 K. Electrical crosstalk between adjacent channels (one on, one off) was quite low. The spot noise at 10 Hz (7 $\mu V/\sqrt{Hz}$), of the CMOS multiplexer operating in the static mode did not vary significantly with operating temperature. In the dynamic mode (3.2-kHz clock) at room temperature, the spot noise at 10 Hz was substantially higher than that measured in the static mode.

1. INTRODUCTION

Although the advantages of having a large number of infrared detectors on the focal plane of an infrared telescope have long been recognized, efficient signal-processing methods for a large number of channels still must be developed. As an example, the multiple-instrument chamber (MIC) of the Shuttle Infrared Telescope Facility (SIRTF) will provide a cryogenically cooled environment for a maximum of six science instruments for astronomical observations (Shuttle Infrared Telescope Facility, Phase A Concept Description, SIRTF Study Office Report, NASA Ames Research Center, Moffett Field, Calif., Aug. 1981). The maximum number of wires between the cold MIC and the warm instrument electronics compartment is to be limited to 1,000, and experience has shown that a minimum number of wires should be brought out of the focal plane. Since several science instruments may require multielement detector arrays or many discrete detectors, on-focal-plane signal processing would have an important role in simplifying the SIRTF system.

Operating under the low background environment of SIRTF, the state-of-the-art infrared detectors are required to have very small noise-equivalent-power (NEP). So, besides possessing the desirable multiplexing capability, the on-focal-plane signal processing unit should have relatively low noise so that the low-level signals from the infrared detectors can be multiplexed out without any significant degradation. In order to evaluate the merit of the CMOS multiplexer (MUX) in low-level signal processing, the noise performance of the CMOS MUX should be better than or comparable to that of a single p-channel MOSFET (ref. 1), a silicon JFET (ref. 2), or a germanium JFET (ref. 3). However, relatively "noisy" multiplexers may still be used to satisfy the less stringent requirements of "housekeeping" data processing.

Various CMOS analog multiplexers have been fabricated and subjected to electrical and environmental testing at room temperature and at elevated temperatures. For example, the 8-channel and the 16-channel CMOS analog multiplexers were designed to be used in high-reliability flight equipment (refs. 4,5). In addition, CMOS monolithic chips have been designed to be used as storage elements and shift registers

in the central processing unit of a digital computer (ref. 6). Previous applications of CMOS multiplexers have encompassed verifications of the CMOS multiplexer, but only when it was operating at room temperature and at elevated temperatures (125°C). Therefore, it is the purpose of this program to understand and demonstrate the performance of the 32-channel CMOS MUX operating at cryogenic temperatures.

The 32-channel CMOS MUX tested in this program was designed and developed by the Irvine Sensors Corporation (formerly, Carson Alexiou Corporation), Costa Mesa, California. This device was designed to operate at temperatures down to about 4 K. The input circuit of each CMOS channel consists of a detector and a load resistor connected to an FET input amplifier.

Under contract to Ames Research Center (NAS2-10136), Irvine Sensors Corporation designed, fabricated, and tested Si:Ga infrared detector assemblies for infrared astronomical applications. The CMOS MUX, developed by the contractor under a separate program, was included as the on-focal-plane signal processing unit for one of the three detector assemblies that were delivered. The CMOS multiplexer approach was selected because of its lower cost and potentially lower noise and power dissipation relative to the commonly used charge-coupled device (CCD) multiplexer.

The objective of the in-house measurements at Ames Research Center was to investigate the noise levels, frequency limits, and temperature effects on the 32-channel CMOS MUX. Measurements were made of (1) the MUX exerciser/drive electronics noise (as a function of clock frequency), (2) single-channel commercial CMOS characteristics, (3) 32-channel CMOS MUX output waveform, and (4) input FET channel gain, leakage current, electrical crosstalk, and noise (as a function of clock frequency). The room-temperature measurements were completed; however, more testing is needed to verify the noise results at liquid-helium temperature and another intermediate temperature.

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2. DESCRIPTION OF THE CMOS MULTIPLEXER

The CMOS MUX was designed to multiplex 32 low-level analog input signals to a single analog output. The CMOS MUX chip layout is shown in figure 1. The device contains 32 analog inputs, a trigger-in (T_{GIN}) and a trigger-out (T_{GOUT}) line, clock ($\overline{CLK}$), power (V+) and ground (V-) lines, voltage-mode output line (V_{out}), and a current-mode output line (I_{ol}). The analog input circuit of each CMOS channel consists of an FET amplifier.

3. CMOS MULTIPLEXER OPERATION

Before the T_{GIN} pulse is applied, the internal clock line ($\overline{CLK}$) is disabled and the I_{ol} line is an open circuit. After the device is triggered, the clock pulses condition the address inputs (V_{SX}) to select sequentially each of the CMOS

channels for signal output. With the addition of an external-source resistor (R_S), signals in the form of current proportional to the output voltage of the input FET will be buffered and sent out to the warm amplifiers via the I_{o1} line. The sequence of operation is shown in the CMOS MUX timing diagram (fig. 2).

To increase the number of available analog inputs, several multiplexers may be operated in tandem by connecting the T_{GOUT} of one MUX to the T_{GIN} of another MUX. After selecting the last channel in the last MUX of the chain, a T_{GOUT} pulse is generated. The I_{o1} line becomes an open circuit, and the internal counter is reset and the internal clock is disabled.

Input Circuit

A block diagram of three typical CMOS channels and their input circuits is shown in figure 3. In our experiment, 3 of the 32 CMOS channels had input circuits connected. The input circuit of one of the "active" channels consisted of a Si:Ga detector and a 10^{10}-Ω load resistor. Each of the other two "active" channels included a pair of Eltec resistors (10^{12} Ω) in the input circuit. This voltage divider provided the gate bias voltage to the input FET, or alternatively, a bias voltage could be applied directly at the gate.

Figure 4 shows the layout of the Si:Ga infrared detector assembly with the input FETs and the CMOS MUX fabricated together as the preamplifier/signal-processing unit. In this figure, only one channel is shown connected to a detector and load resistor.

4. CMOS MULTIPLEXER EXERCISER/DRIVE ELECTRONICS

When the CMOS channel is turned on, the FET in the input circuit acts as a source-follower amplifier. Using an externally controlled CMOS switch for manual clocking, all CMOS channels can be turned on individually and kept on one at a time; this is referred to as the static mode. The I_{o1} line is grounded and the output circuit is connected to V_{out} (shown in fig. 3). Dynamic mode refers to the clocking of the CMOS MUX with a pulse generator at various desired clock frequencies. In this mode, the I_{o1} line is connected to the virtual ground input of an inverting operational amplifier. The output signal is then processed through a second- and a third-stage operational amplifier, a fast sample and hold, and a slow sample and hold (S/H). The fast S/H "digitizes" the analog output signal from the third-stage operational amplifier. While the output signal of each CMOS channel is being held by the fast S/H, the slow S/H, together with a thumbwheel switch, is used for demultiplexing the output signal of each channel. Figure 5 shows the block diagram of the CMOS MUX exerciser/drive electronics.

Initial noise measurements on the CMOS MUX operating with its drive electronics showed the noise to be dominated by the drive electronics noise. Large-amplitude noise was found on both the signal lines and the power lines; shields on the coaxial cables were not connected properly. The MUX exerciser/drive electronics was then modified. The main feature of the modification was that the analog and digital sections were put on separate printed circuit boards. Each had a separate ground line. A battery power supply was used to operate the analog and digital sections to avoid 60-Hz interference. Optoisolators were used between the digital and analog sections to control the sample and holds.

5. DRIVE ELECTRONICS NOISE

Test Setup

The test setup for the drive electronics noise measurement is shown in figure 6. A Wavetek wave generator was used to provide clocking for the CMOS MUX. The value of the drive electronics input resistor R_0 was selected to simulate the input FET channel resistance of one of the 32 CMOS MUX channels. The effective first-stage gain (from R_0 to the output of the first-stage operational amplifier) could be arbitrarily chosen by using appropriate values for R_0 and the first-stage feedback resistor. An offset potentiometer in the circuit was used to zero the output voltage of the first stage operational amplifier before each noise measurement. The limiting amplifier bandwidth in the drive electronics was 17.7 kHz at the first stage. Noise from the slow sample and hold output was fed into the Ithaco 1201 low-noise preamplifier. The drive electronics noise was amplified above the noise floor level of the Nicolet Model 446A FFT spectrum analyzer. The spectral noise voltage density was then plotted with a HP 7004A X-Y recorder, and the plotted spectral noise voltage density was gain-corrected and referred to the grounded input of the R_0 resistor.

Results Before Modification

The static noise of the drive electronics was measured at the third-stage operational amplifier output (fig. 7). The input-referred noise spectrum contained 1/f and $1/\sqrt{f}$ noise components, probably a result of amplifier output drifts. The drive electronics noise level should be dominated by the first-stage operational amplifier (OP 08) with spot noise of 22 $nV/\sqrt{Hz}$ at 10 Hz (from PMI Databook). As we can see from figure 7, the static noise of the drive electronics is about 10 times higher than expected.

The spectral noise voltage densities of the MUX exerciser (drive electronics) for clock frequencies of 2.5 kHz, 5 kHz, and 25 kHz are shown in figures 8, 9, and 10, respectively. A common characteristic of these noise spectra is the $(\sin x)/x$ minima, located at the sampling frequency f_s and at the multiples of f_s. For this MUX exerciser, the sampling frequency is defined as

$$f_s = f_c/40 \tag{1}$$

where f_c is the frequency of the clock pulses fed into the MUX by the exerciser. The internal counter of the CMOS MUX resets after 40 clock pulses. The spikes seen at the $(\sin x)/x$ minima are due to pickup from 60-Hz ripples aliased into the Nyquist bandwidth of the sample and hold circuits.

The fast S/H in the MUX exerciser samples the analog output from the third-stage operational amplifier and holds the sampled output amplitude from each MUX channel until it is updated $1/f_s$ seconds later. Meanwhile, the noise level or signal at each channel can be measured from the slow S/H output. According to reference 7, convolving the Fourier transform of an infinite-length sample with a "boxcar" $(\sin x)/x$ function is equivalent to having a sample of finite record length. So, the output waveform has the form

$$V_n(f) = E_n(f)\sin(\pi f/f_s)/(\pi f/f_s) \tag{2}$$

where $E_n(f)$ is the spectral noise density. The broadband rms noise amplitude in the frequency range from 0 to f_s is

$$V_{nRMS} = \left\{ \int_0^{f_s} [E_n(f)\sin(\pi f/f_s)/(\pi f/f_s)]^2 \, df \right\}^{1/2} \quad (3)$$

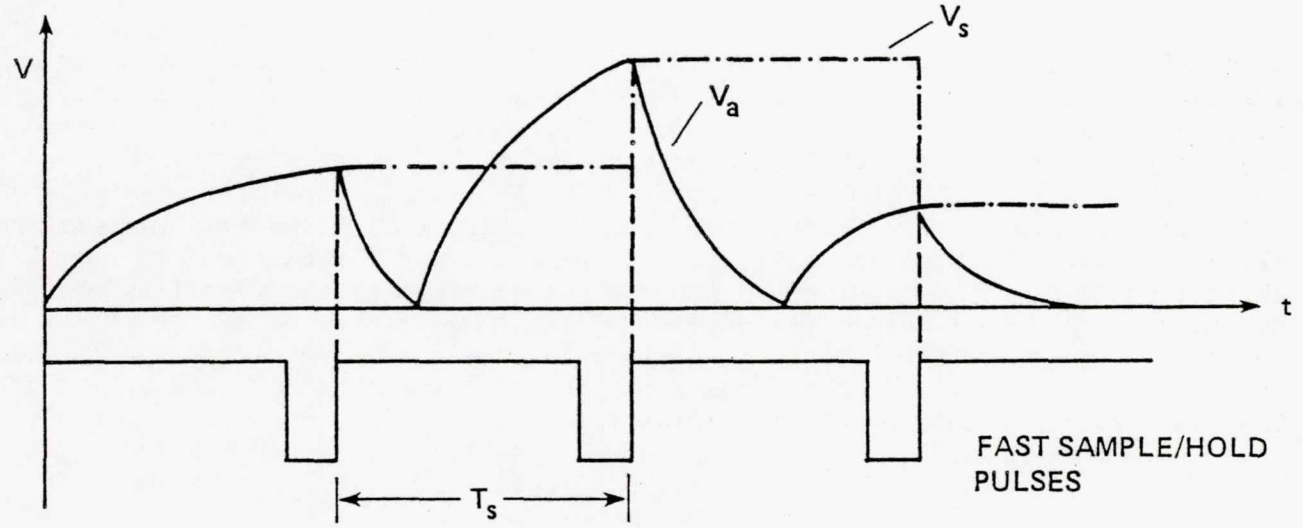
Results After Modification

The spectral noise densities of the modified MUX exerciser/drive electronics are shown in figures 11 and 12. Operational amplifier noise (fig. 11) at 10 Hz was reduced to 50 nV/$\sqrt{\text{Hz}}$. In Figure 12, the spot noise at 10 Hz seemed to be about 600 times lower than the noise level before modification (fig. 9). However, the total amplifier gain in figure 9 was only 5, whereas the total amplifier gain in figure 12 was 10,000. This led us to believe that in figure 9, the inherent noise in the operational amplifiers was not raised sufficiently above the inherent noise in the fast and slow sample and holds. The gain-corrected, input-referred noise level shown in figures 8-10 may have included S/H noise, as well as operational amplifier noise.

Amplifier Bandwidth Adjustment

It is significant that for the same amplifier bandwidth, the white-noise portion of the spectral density is inversely proportional to the clock frequency, f_c (ref. 8). Since sampling transposes the total noise power into the baseband (0 - $f_c/2$), a system operating at a higher clock frequency will have a lower spectral density. This can be verified in figures 8-10 where the limiting amplifier bandwidth used was 17.7 kHz for all three cases. However, it will be shown in the following explanation that the required amplifier bandwidth for a given sample and hold accuracy is proportional to the clock frequency. So, the white-noise portion of the spectral density might be independent of clock frequency if the amplifier bandwidth were adjusted accordingly.

Sketched below are the amplifier analog output signal V_a and the sample and hold output signal V_s.



We know that $V_a = V(1 - e^{-t/\tau})$ and that $V_s = V(1 - \varepsilon)$, where V is the maximum amplitude of the analog signal, T_s is the sampling time interval, τ is the RC time-constant of the amplifier, and ε is the accuracy. Setting $V_a = V_s$, we have

$$t/\tau = -\ln \varepsilon \tag{4}$$

We need to determine the required amplifier bandwidth, $\Delta f = 1/(2\pi\tau)$ so that the desired accuracy can be achieved. For $t = T_s = 1/f_s = 40/f_c$, we get

$$\tau = 40/(-f_c \ln \varepsilon) \quad \text{or} \quad \Delta f = (-f_c \ln \varepsilon)/(80\pi) \tag{5a}$$

Equation (5) determines the appropriate amplifier bandwidth for a given clock frequency and accuracy. The fast S/H (Teledyne Philbrick 4855) that we used in this experiment has an accuracy of 0.01% for frequencies up to 194 kHz. So equation (5) becomes

$$\Delta f = 0.0366\, f_c = f_c/27.3 \tag{5b}$$

However, the cutoff frequency of the amplifier according to equation (5b) is greater than the sampling frequency ($f_s = f_c/40$), and some information may become lost owing to aliasing error. Therefore, it is preferable to place a low-pass filter with a cutoff frequency equal to one-half the sampling frequency at the input of the sample and hold. If, for example, the detector signal is chopped at a maximum rate of 20 Hz, then, using a low-pass filter implies that the multiplexer must operate at clock frequencies greater than or equal to 5 kHz (see fig. 9) to avoid signal attenuation.

It should be noted that the cutoff frequencies of the amplifier used throughout the experiment were larger than the sampling frequency. We know that the greater the amplifier bandwidth, the greater the total output noise. If we assume that the voltage gain is unchanged, and the amplifier bandwidth for each clock frequency is the same as the sampling frequency, then the "corrected" spot noise at 10 Hz extracted from figures 8-10 appears to be independent of the clock frequency (see table 1). The white-noise portions of the noise spectrum, after correction, are 4.37 $\mu V/\sqrt{Hz}$, 5.14 $\mu V/\sqrt{Hz}$, and 4.79 $\mu V/\sqrt{Hz}$ for clock frequencies of 2.5 kHz, 5 kHz, and 25 kHz, respectively.

6. SINGLE-CHANNEL COMMERCIAL CMOS CHARACTERIZATION

Test Setup

The 32-channel CMOS MUX was fabricated with units virtually identical to a commercial CMOS package. One CMOS unit and an FET input stage were connected and tested on a breadboard. The setup is shown in figure 13. Two 1-MΩ resistors were used to simulate a load resistor and a detector at the input of the FET amplifier. The substrates of the p-channel MOSFETs were connected to the source of the p-channel MOSFETs (V_{out}) and those of the n-channel MOSFETs were also connected to the source of the n-channel MOSFETs (V_{ss}). Gain and noise measurements were made in the source-follower mode with V_{ss} grounded and output obtained at V_{out}. The on/off operation of the CMOS was controlled by the applied voltage at V_{sx}, either 10 V or ground. The current measured at V_{ss} with a Keithley 601B electrometer connected in series to the CMOS channel is the leakage current of the CMOS when it is turned off. All of the measurements were done at room-temperature.

FET Channel Gain

The FET channel gain or voltage gain of the FET amplifier was obtained from the slope of the V_{out} versus V_{gate} plot in figure 14. The device was linear for $0.5\ V \le V_{gate} \le 7.3\ V$. The average voltage gain was calculated to be 0.80. The voltage gain of a source-follower amplifier circuit can be represented by (ref. 9)

$$A = V_{out}/V_{gate} = [(g_m + j\omega C_{sg})R_s]/[1 + (g_m + g_{ds} + j\omega C_{sg})R_s] \qquad (6)$$

where g_m is the FET channel transconductance, C_{sg} is the gate-to-source capacitance, g_{ds} is the drain-to-source shunt conductance, R_s is the source resistor, and ω is the angular frequency.

At low frequencies or for the static case, the gain is, approximately,

$$A = (g_m R_s)/[1 + (g_m + g_{ds})R_s] \qquad (7)$$

Since g_{ds}, the drain-to-source shunt conductance, is usually small, we see that A approaches unity as R_s becomes very large. However, R_s is usually selected for a desired range of linearity of the input/output characteristics. If we neglect g_{ds}, using $A = 0.8$ and $R_s = 10\ k\Omega$, the FET transconductance is calculated to be 400 μmho.

The transconductance g_m varies with the difference between the gate voltage and the threshold voltage. However, the effect of g_m on A is only minor. The gate voltage V_g was varied from 0 V to 6.85 V for the linear region in figure 14; the measured drain current varied from 600 μA to 100 μA. The manufacturer of the commercial CMOS states that $g_m = 400$ μmho at 100 μA drain current. (Personal communication from L. Wall, Irvine Sensors Corporation, Costa Mesa, Calif.) Then, for the device operating in the saturation region, $g_m = 0.04\sqrt{I_{DS}}$ (see Static Noise, sec. 8). So, for the linear region in figure 14, the FET channel gain A only varied from 0.91 (at $V_g = 0$ V) to 0.8 (at $V_g = 6.85$ V).

The voltage gain can be indirectly attenuated by a "body effect" parameter (ref. 10) which seems to depend on the source-substrate reverse bias voltage; its value is no greater than 1. Normally, an FET with zero source-substrate bias would result in a lowest threshold voltage at a given operating temperature. So increasing the magnitude of the source-substrate bias tends to increase the threshold voltage V_{th} of the FET. Since g_m is proportional to $(V_{gs} - V_{th})$, applying a source-substrate bias will give a smaller g_m at the same V_{gs}. Consequently, gain A will be smaller if there is a source-substrate bias. For the 32-channel CMOS MUX, the substrates of all the MOSFETs were not connected to the source.

Leakage Current

The drain currents through the input FET were measured for different gate voltages when the CMOS unit was turned on. The measured drain currents varied from 1.5 μA (at $V_g = 8.7$ V) to 600 μA (at $V_g = 0.01$ V). The drain current I_{DS} decreased from 1.8 nA at $V_g = 9$V to 15 pA for $V_g > 9.5$ V. This demonstrated the input FET cutoff condition when $|V_{gs}|$ was less than the threshold voltage; $|V_{th}|$ was estimated to be about 1 V at room temperature. The current measured with $V_g > 9.5$ V could be considered as the subthreshold current.

When the CMOS unit was turned off, the measured leakage current through the off channel was 1.7 pA. From the manufacturer's specification (ref. 11), the typical

device quiescent direct current is about 5 nA for three CMOS pairs. The measured value is about three orders of magnitude lower than the manufacturer's specification; there is no plausible explanation for this discrepancy.

Noise

The spectral noise voltage density of the commercial CMOS single-channel simulation (one CMOS unit and an input FET) is shown in figures 15 and 16. The spot-noise level appeared to be higher when the CMOS channel was turned on (fig. 15). Most likely, the input FET contributed additional noise when the CMOS was in this state. The noise voltage varied (as $1/\sqrt{f}$) from 2.5 Hz to 13 Hz when CMOS was on and from 2.5 Hz to 25 Hz when it was off.

7. CMOS MULTIPLEXER: ORIGINAL DRIVE ELECTRONICS

Output Waveform

The multiplexed output waveforms of the three active channels, 18, 19, 20, are shown in figures 17(a), 17(b), and 17(c), respectively. The measurements were made at room-temperature and the clock rate was 5 kHz. A bias voltage of 3.84 V was directly applied at the gate of each of the active channels. The output waveform was obtained at V_{out} with V_{ss} grounded (voltage mode). The "fixed pattern" noise of the "inactive" channels is quite evident in figure 17. The gates of the "inactive" channels were neither biased nor grounded.

The MUX output waveform operating at 4.9 K is shown in figure 17(d). The "fixed-pattern" noise seems to be less than that at room-temperature. It is peculiar that the overall output levels of the inactive channels tended to slope down from both sides toward the three active channels. This is not noticeable in the room-temperature output waveforms.

The response of the "active" channel source-follower output V_{out} to changes in the gate voltage was dependent on the RC time-constant. We see (refer to fig. 20) that R would be the effective resistance of R_D and R_L at the input FET gate and C would be the input capacitance of the FET. For channels 18 and 20, R_D and R_L were approximately equal (of the order of 10^{11} to 10^{12} Ω). Therefore, the maximum applied gate voltage would be about 5 V from a 10 V bias. In order to get a gate-voltage range of 0 to 10 V, we either connected a bias supply directly to the gate or connected a 1-MΩ resistor in parallel with the resistor R_D. The bias supply reduced the effective resistance at the input FET gate; however, a lead which had to be brought out from the gate to the bias supply circuit contributed extra capacitance. Nevertheless, the response time was still very short. If bias voltage was applied across both the R_D and R_L without employing the aforementioned biasing schemes, the RC time-constant would certainly increase.

FET Channel Gain: Static

For the static mode, both dc and ac methods could be used in measuring the FET channel gain or voltage gain A. In the dc method, A is defined as $\Delta V_{out}/\Delta V_{gate}$. So, varying the gate bias voltage by a small amount will produce a proportional change at the source output of the input FET amplifier; V_{out} could then be monitored using either an oscilloscope or a voltmeter. For the ac method, we could set a dc gate bias voltage and simultaneously apply a small sine wave at the gate of the input FET. As a

result, A could be calculated from the ratio of the peak-to-peak V_{out} to peak-to-peak V_{gate}.

As mentioned previously (FET Channel Gain), the effect of gate bias voltage on the voltage gain is rather insignificant, and the average voltage gain for different values of V_{gate} was calculated from the slope of the linear region of the best-fitted curve in figure 18.

The room temperature FET channel gains for channels 18 and 19 with a 10-kΩ source resistor were calculated to be 0.53 and 0.49, respectively. This result is lower than the voltage gain of the input FET for the single-channel commercial CMOS by about 36%. We can estimate the "body effect" parameter to be 0.64. Since the substrate and the source of the input FET were not tied together, we expect that A would be somewhat reduced by the "body effect." We also notice that channels 18 and 19 were linear over the range of gate voltages from 0 to 5 V, whereas the single-channel commercial CMOS was linear up to 7.5 V. If we consider that the cutoff region occurs where the curves in figures 14 and 18 start to level off, we can estimate the threshold voltages to be -1 V for the input FET used in the commercial CMOS circuit, -0.67 V for channel 18, and -2.2 V for channel 19. However, the substrate "body bias" effect should not be the sole cause of the discrepancy in V_{th}; differences in the charge concentrations in the surface states and oxide, and in doping concentrations between the commercial CMOS and 32-channel CMOS MUX, might result in different output characteristics.

The input FET amplifier channel gain for channels 18 and 19 of the CMOS MUX operating at a temperature of 4.9 K was calculated to be 0.63 (fig. 18). The linear region spanned from gate voltage of 0 to 8 V, and V_{th} was estimated to be -1.9 V. The magnitude of V_{th} increases as temperature decreases. For nonpolar semiconductors, such as Si, the mobility of the carriers μ varies as $T^{-3/2}$ (ref. 12). Since the transconductance g_m is proportional to the effective surface mobility μ_n (where, $\mu_n \approx 1/2\ \mu$ at room temperature) and $(V_{gs} - V_{th})$, the increase in μ_n at low temperature offsets the decrease in $(V_{gs} - V_{th})$, causing g_m to increase. It has been observed that at 4.2 K, the channel hole mobility is 3 to 4 times greater than that at room temperature, and the transconductance increases correspondingly (ref. 13).

Figure 19 shows a plot of V_{out} versus V_{gate} for different values of source resistance R_s. As mentioned in section 6 (FET Channel Gain), we find that the FET channel gain increased as R_s was made larger. Notice that different MUX channels (20-22) were used in the measurement because of broken signal wires to the gate contacts of channels 19 and 20.

FET Channel Gain: Dynamic

The input FET channel gain could also be measured when the MUX is operating in the dynamic mode. The FET channel gain was again measured using the dc method. As in the static mode, a change in the gate voltage resulted in a proportional change in the source voltage V_{out}. Rather than having a constant dc level at V_{out}, as in the static mode, the output waveform was similar to that shown in figure 17 when the source output voltages of the 32 channels were multiplexed out. However, only the active channel in the MUX would respond to the gate voltage. As the clock frequency was decreased to less than 32 Hz, a storage oscilloscope was required to measure the output source voltages. This sometimes led to inaccurate readings off the oscilloscope.

Output characteristics, V_{out} versus V_{gate}, of channels 19 and 20 were measured at room temperature with R_S = 10 kΩ, for clock frequencies of 4,800, 480, 48, and 4.8 Hz. The results were not significantly different from the static case, as shown in figure 19.

The average FET channel gain of channels 18 and 19 operating at T = 4.9 K and at clock frequencies of 3,200, 320, 32, and 3.2 Hz, was calculated to be 0.60 (fig. 18). This value is not much different from that obtained in the static mode. From this we can conclude that the FET channel gain is slightly higher at liquid-helium temperature, but it is independent of clock frequency.

Leakage Current

The MUX leakage current was measured at room-temperature and at 4.9 K. Two different methods were used. In both cases, a CMOS switch was used to manually clock past all 32 channels of the MUX, thus ensuring that all the channels were turned off. One method was to measure the voltage drop across the source resistor R_S (with a Keithley 601 electrometer). Assuming that all 32 channels leak evenly, the leakage current per channel is defined as $i_L = \Delta V/(32R_S)$. This method measured the junction leakage current across the input FET amplifier and the p-channel MOSFET of the CMOS unit. The second method used was to connect the electrometer in series with the n-channel MOSFETs at the point V_{ss} (fig. 20). The leakage current per channel is obtained by dividing by 32, the current measured directly with the electrometer. This method measured the leakage current of the device that was off, the n-channel MOSFET. At room-temperature, the leakage current was 3.2 μA/channel for the first method and 0.9 μA/channel for the second. This is quite comparable to the maximum limit (1 μA at 25°C) as specified by the manufacturer of the commercial CMOS (ref. 11). At T = 4.9 K, the leakage current was 61 nA/channel for the first method and 0.23 pA/channel for the second. The wide discrepancy in the results obtained by the two methods is still unresolved.

Electrical Crosstalk

The electrical crosstalk measurement was designed to determine how the input signal at an off channel would affect the output signal from an adjacent on channel. This test was performed in the static mode with one channel turned on and the others turned off. A small-amplitude sine wave was applied at the input FET gate of the off channel. The crosstalk voltage was then measured at V_{out} of the on channel with an oscilloscope. Channel 20 was turned on and the input FET was biased to about 100-μA drain current. The measured crosstalk from channels 18 and 19 at room-temperature operation was about 0.2%. The crosstalk was defined as the ratio of the crosstalk peak-to-peak voltage to peak-to-peak voltage of the input sine wave.

Later, a similar crosstalk measurement was done using a Nicolet 446A spectrum analyzer instead of an oscilloscope. First, the spot-noise voltage ($V/\sqrt{Hz}$) at 20 Hz was measured at V_{out} of the on channel with a 20-Hz sine wave applied at the gate of the off channel. Then, the spot-noise voltage at 20 Hz was measured at V_{out} of the on channel with the same sine wave applied at the gate of the on channel. The ratio of the two values obtained was defined as the electrical crosstalk. Channel 18 was turned on, and the V_{gs} was about -4.5 V. The crosstalk from channels 19 and 20 was measured to be 0.55% with the MUX cooled to 4.9 K. The set of crosstalk measurements at room temperature and at 4.9 K was not completed.

It is conceivable that electrical crosstalk can be measured with the MUX operating in the dynamic mode. Similarly, we would apply a sine wave at the gate of one channel and measure the crosstalk from the slow S/H output of an adjacent channel. Again, we can monitor the crosstalk voltage with either an oscilloscope or a spectrum analyzer. However, this set of measurements was not performed.

Noise

Figure 20 depicts the noise test setup for the CMOS MUX operating in the dynamic mode. For the noise measurement of the CMOS MUX operating in the static mode, the Nicolet spectrum analyzer was connected to V_{out}, as shown in figure 20. Since we wanted to measure the spectral noise density referenced to the gate of the input FET amplifier, we had to determine the effective first-stage operational amplifier gain G in the analog circuit. Gain G was measured with the MUX operating in the static mode. By imposing a sine wave at the input FET gate of an active channel and measuring the first-stage operational amplifier peak-to-peak output voltage, G was determined from the ratio of the first-stage output p-p voltage to the applied p-p voltage at the input FET gate. By offsetting the dc voltage at the first-stage output to ground, we determined the current flowing through the summing junction at V_{ss}, which was equivalent to the drain current I_{DS} through the input FET. The effective first-stage operational amplifier gain could be defined as follows:

$$G = R_{FB1}/(1/g_m + R_s) \tag{8}$$

where R_S is the source resistor and R_{FB1} is the feedback resistor of the first-stage operational amplifier. The output impedance of the input FET when turned on is $1/g_m$.

Figures 21 through 24 represent the spectral noise density of channel 18 of the MUX while operating in the static and dynamic modes at 4.9 K. The spot noise at 10 Hz is about 7 $\mu V/\sqrt{Hz}$ (fig. 21). This value is within the range of 1 to 11 $\mu V/\sqrt{Hz}$ measured on a similar FET (ref. 14). The range of spot-noise values obtained was for FETs with n-type substrate resistivity from 0.22 to 3.0 ohm cm. The substrate resistivity of the CMOS MUX input FET amplifier is not available. The results from figures 22 to 24 (dynamic mode) are unreliable because the noise levels measured on the MUX exerciser/drive electronics later were found to be slightly lower than those measured on the MUX. This implies that the MUX exerciser contributed a significant portion of the noise to those shown in figures 22-24. The noise spectrum level of the MUX exerciser was found to be 3 times higher than when initially measured (see fig. 8). This difference was later traced to the noise pickups from the drive electronics grounding problems and broken shield wires on the wiring harnesses.

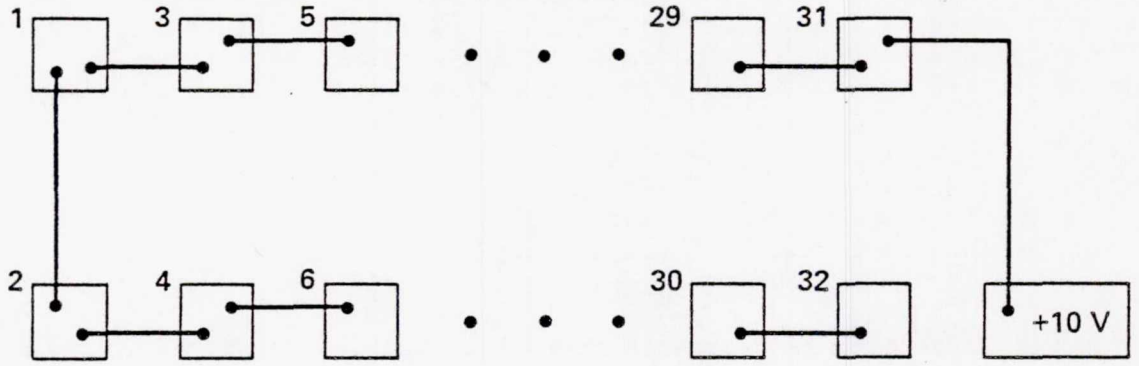
Similarly, note that noise levels appeared to be higher as the clock frequency decreased. However, as was pointed out in section 5 (Amplifier Bandwidth Adjustment), spot-noise level should be independent of clock frequency if the warm amplifier bandwidths were adjusted accordingly. The static mode and the 3.2-kHz clock noise plots of channel 18 exhibited $1/f$ and $1/\sqrt{f}$ components at low readout frequencies.

With the input FET gate voltage at 3.0 V, the measured effective first-stage operational amplifier gain was 0.6. The drain current was calculated to be approximately 14 μA, which indicated that the input FET was probably operating in the neighborhood of the weak inversion region.

8. CMOS MULTIPLEXER: MODIFIED DRIVE ELECTRONICS

Output Waveform

An attempt was made to minimize the fixed-pattern noise of the CMOS MUX by stitch-bonding all the gates of the "inactive" channels together to a 10-V supply. We would expect the output of the "inactive" channels to be at 9V. However, as seen in figure 17(f), the output of the odd-numbered channels remained at 9 V while the even-numbered channels were at 3 V. This inconsistency was later determined to be caused by a bad channel, channel 32. It appeared that there was some kind of leakage which caused the gate of channel 32 to stay at ground potential. Therefore, the output voltage of the even-numbered channels was at 3 V as shown. According to the MUX chip channel layout as sketched below, all the channels should have been tied to 10 V. Somehow, the wire bond between pad 1 and pad 2 might not have been adequately secured so that the top and bottom rows of CMOS channels were electrically isolated from each other (see sketch below). Note that the output of channel 17 was affected by leakage. However, when the MUX was cooled to 77 K, channel 17 behaved normally (fig. 17(g)). Later, after repairing some broken wire bonds, channels 20, 21, and 22 were chosen to be the "active" channels instead of channels 18, 19, and 20.



Static Noise

For a MOSFET operating in the saturation region ($|V_{DS}| > |V_{gs} - V_{th}|$), the equations for the drain current I_{DS} and the transconductance g_m are given below (ref. 10):

$$I_{DS} = \mu_n C_o Z(V_{gs} - V_{th})^2/(2L) \tag{9}$$

$$g_m = \mu_n C_o Z(V_{gs} - V_{th})/L \tag{10}$$

where μ_n is the effective surface mobility, C_o is the oxide capacitance, Z is the channel width, and L is the channel length. Combining equations (9) and (10), we get

$$g_m = (2\mu_n C_o Z I_{DS}/L)^{1/2} \tag{11}$$

The manufacturer (Irvine Sensors Corporation) of the CMOS MUX quoted that $g_m = 400$ μmho for $I_{DS} = 100$ μA under room-temperature operation. Assuming that μ_n and C_o are constant with gate voltage, we get for the saturation-region operation,

$$g_m = 0.04(I_{DS})^{1/2} \tag{12}$$

Actually, μ_n is not constant, and this introduces second-order effects into the MOSFET analysis (ref. 10). The surface mobility of the MOSFET is about one-half the bulk mobility. For given device parameters, an increase in μ_n will increase I_{DS} and g_m. It is understood that μ_n decreases as V_{gs} is increased above the threshold voltage V_{th}. This is due to the reduced scattering and strong attraction of carriers at the silicon-oxide interface under high gate biases. The surface mobility μ_n reaches a maximum as the value of V_{gs} approaches the value of V_{th}. Then, μ_n decreases drastically as $|V_{gs}| < |V_{th}|$, which is the weak-inversion region. In this state, the MOSFET channel is weakly inverted because the surface potential is less than the bulk potential.

In our experiment, I_{DS} was obtained by noting the offset voltage required to zero the first-stage operational-amplifier output. The drain current I_{DS} is defined as V_{offset}/R_{offset} (fig. 20). If the MOSFET was not operating in the linear or triode region ($|V_{DS}| < |V_{gs} - V_{th}|$), then g_m could be calculated from reference 10. Also, g_m could be obtained indirectly from the measured effective FET channel to first-stage operational-amplifier gain G for a selected I_{DS}. Therefore, from equation (8),

$$g_m = G/(R_{FB1} - GR_s) \tag{13}$$

Alternatively, measuring the FET channel or voltage gain A in the source-follower mode would also give us g_m from equation (7),

$$g_m = A/[R_s(1 - A)] \tag{14}$$

Since the MOSFET transconductance is defined by

$$g_m = (\partial I_{DS}/\partial V_{gs}) , \quad V_{DS} = \text{const} \tag{15}$$

a more direct way of obtaining g_m would be to measure the change in drain current I_{DS} for a minute change in V_{gs}, with V_{DS} held constant. Although this method seems to be more preferable to the indirect method, it was not used in the experiment. A more accurate measurement technique can be used to determine both g_m and g_d (drain conductance) in a single circuit. It is based on the principle of null indication and, therefore, avoids the absolute measurement of the small input and output signal voltages (ref. 15).

For room-temperature operation, g_m was calculated from equation (13) to be 40 μmho after G was measured at I_{DS} = 100 μA. This value was 10 times smaller than the g_m quoted by the manufacturer. However, the uncertainty of the second-order effects in the device and the degree of accuracy of the indirect method make the value of the calculated g_m questionable. The transconductance g_m at other operating temperatures was not obtained.

Figures 25-27 present the spectral noise density of the "inactive" channels (fig. 25), and "active" channels 21 (fig. 26) and 22 (fig. 27). All the measurements were performed while the MUX was operating at room temperature and in a static mode. In the static mode, noise was measured at the source of the input FET. The measured spectral noise density from the spectrum analyzer output was gain corrected, using the voltage gain A, and referred to the gate of the input FET amplifier. In figure 25, channels 24 and 25 were the "inactive" channels tied to 0 and 10 V, respectively, at the gate. Since the FET channel gain A could not

be measured, A was assumed to be 0.78 for both channels 24 and 25. The spot noise for the inactive channels is about 3 to 4 times lower than that for the active channels, This finding could not be ascertained because the FET channel gains of channels 24 and 25 were not measured.

The calculated drain currents for the cases shown in figures 25-27 were all less than 10 μA. Drain current I_{DS} was calculated using equations (12) and (14). Typically, the measured value of V_{th} is based on a customary arbitrary value of I_D (10 μA). So, we can consider the drain current of the FETs operating in the weak-inversion region to be less than 10 μA. Comparing the overall noise levels with figure 15 (FET from commercial CMOS at I_{DS} = 280 μA), we see that the noise of the FET operating in the weak-inversion region is about 40 times higher than that operating in the strong-inversion region. According to Hosticka (ref. 16), white-noise voltage spectral density of the MOSFET in the weak-inversion region is higher than that in the strong-inversion region, and 1/f noise remains the same. In the strong-inversion region, the white-noise component is due to the thermal channel noise; in weak inversion, it is the shot noise caused by diffusion current (ref. 17).

Theoretically, we would expect to see the room-temperature Johnson noise of the effective resistance (load resistor in parallel with the detector) at the gate of the input FET circuit of each channel. However, as shown in table 2, Johnson noise from channel 21 is negligible in comparison with the FET noise. As for channel 22, the noise bandwidth for the input FET circuit is so small that the Johnson-noise contribution is insignificant.

Dynamic Noise

The following discussion and results on dynamic-mode noise measurements are preliminary because of suspected noise coupling between the digital and analog sections of the MUX exerciser/drive electronics. Because of limited test time, this uncertainty could not be resolved.

Spectral noise densities of the CMOS MUX operating at room temperature and at 3.2-kHz clock are shown in figures 28 and 29. The waveforms have the characteristics of a $(\sin x)/x$ function as expected. Before the noise measurements were made, the effective FET-channel-to-first-stage gain G was obtained for channels 21 and 22 at V_g between 0 and 8.2 V. Theoretically, G should vary with V_{gs}. However, since the high source resistance (100 kΩ) reduced the drain-to-source current I_{DS}, the input FET was forced to operate in the weak-inversion region. It was found that the measured G did not decrease noticeably as the magnitude of V_{gs} was reduced. Therefore, G = 60 for channel 21 and G = 77 for channel 22 were used to reference the measured noise to the input FET operating at different V_{gs}. The drain currents I_{DS} for channels 21 and 22 were 0.14 μA and 0.7 μA, respectively.

Figures 28 and 29 illustrate the effect of V_{gs} on the noise levels. However, because of the inconsistency of the result between figures 28 and 29, we could not suggest a relationship between the spot noise and V_{gs}. For channel 21 operating in the weak-inversion region (fig. 28), the spot noise at 10 Hz is between 18 $\mu V/\sqrt{Hz}$ to 40 $\mu V/\sqrt{Hz}$, or between 1.15 $\mu V/\sqrt{Hz}$ to 2.56 $\mu V/\sqrt{Hz}$ if the amplifier bandwidth cutoff is reduced to the value of the sampling frequency. Figure 29 shows the noise level for the input FET operating in a cutoff mode (V_{gs} > 0 V). Electrons accumulated in the channel and no inversion layer was formed. The FET behaved as two p-n diodes, shutting off the current flow through the channel. The expected noise sources would be due to gate leakage currents. Theoretically, g_m should be very

low in the vicinity prior to cutoff. Therefore, the correct G to use would be so small that it might even be difficult to obtain an accurate measurement of G with our test setup. It was not clear what value of G should be used. As a result G = 77 was used for the V_{gs} = +1.0 V case. We found that the noise in the FET cutoff case is limited by the grounded input noise of the drive electronics.

Notice that the grounded input drive electronics spot noise at 10 Hz is now 50 times higher (fig. 29) than that measured just after the drive electronics was modified (fig. 12). The total amplifier system gain used now was 77 versus 10,000 for the case shown in figure 12. An initial attempt to explain this discrepancy would be to claim that the system gain used in figure 29 was not large enough to raise the noise at the input of the fast S/H sufficiently higher than the inherent noise of the fast S/H. However, this was not the case because the gain enhanced input noise to the fast S/H was 90 $\mu V/\sqrt{Hz}$ at 10 Hz and the inherent fast S/H noise was 25 $\mu V/\sqrt{Hz}$ at 10 Hz. Subtracting off the contribution from the inherent fast S/H noise would give us 86 $\mu V/\sqrt{Hz}$ at 10 Hz; that is, the drive electronics might have degraded with time.

Later, various source resistors less than 100 kΩ were used in order to allow the MUX to operate in the saturation region (10 μA ≤ I_{DS} ≤ 400 μA). The effective FET-channel-to-first-stage-operation-amplifier gain G was measured for each selected I_{DS}. As expected, G increases with $|V_{gs}|$. Figure 30 illustrates the linearity of the input FET for various combinations of source and first-stage feedback resistors. We see that using a 10-kΩ source resistor provided the greatest dynamic range and also enabled the FET to operate in the strong-inversion and saturation region.

Figure 31 shows that the spectral noise density of the CMOS MUX (channel 21) operating in the strong-inversion region is relatively independent of the drain current and of V_{gs}. The 1/f or $1/\sqrt{f}$ noise components are not noticeable in the plot. The spot noise at 10 Hz is about 100 $\mu V/\sqrt{Hz}$, or 6.72 $\mu V/\sqrt{Hz}$ if amplifier bandwidth is reduced to 80 Hz (sampling frequency) (see table 3). In spite of the higher grounded input drive electronics noise, the measured noise is still CMOS-MUX-noise dominant.

Noise Dependence on Clock Frequency (Room Temperature)

Note that this CMOS MUX system has essentially two contributing noise sources, namely, Johnson noise, owing to the effective resistance of R_D and R_L, and the noise of the CMOS MUX. The bandwidth of the input FET circuit is $1/(2\pi R_{eff}C)$ where R_{eff} is the effective resistance and C is the FET input capacitance. Table 2 presents the bandwidths and Johnson noise of the input circuit at various temperatures. The CMOS MUX noise spectrum has the characteristics of $(\sin x)/x$ minima, and a white-noise portion at approximately $f < f_s/2$ where f_s is the sampling frequency. If we assume that the CMOS MUX noise bandwidth is the same as the MUX exerciser amplifier bandwidth, then the CMOS MUX noise bandwidth would vary as we adjust the exerciser amplifier bandwidth accordingly with the clock frequency used.

The spectral noise densities for the CMOS MUX operating at various clock frequencies are shown in figures 28 and 29 and in figures 32-37. Since the amplifier bandwidth (BW) used (19.4 kHz) was larger than that required for each of the clock frequencies used in figures 28 and 29 and 32-37, the measured in-band rms noise should be reduced by a "bandwidth adjustment reduction factor" which we would define as

$[(\text{BW from dc to the sampling frequency})/(19.4\ \text{kHz})]^{1/2}$

A sample of the corrected spot noise at various readout frequencies for channels 21 and 22 is shown in table 3. Spot noise measured at different clock frequencies could only be reasonably compared if the readout frequency being considered is much less than the sampling frequency at which the $(\sin x)/x$ minimum occurs. Therefore, from table 3, if we compare the 3,200-Hz case (fig. 29) with the 320-Hz case (fig. 33) at readout frequencies between 1 and 2.5 Hz, and the 32-Hz case (fig. 35) with the 320-Hz case at readout frequency of 0.2 Hz, we find that the corrected spot noise is independent of clock frequency.

Figures 38 and 39 show the reconstructed CMOS MUX noise spectra after the "bandwidth adjustment reduction factor" was applied to the original noise spectra. For channel 21 (with detector), Johnson noise from the effective resistance is still negligible, and the white-noise components of the "bandwidth-corrected" CMOS MUX noise spectra range from 1.16 $\mu V/\sqrt{Hz}$ to 6.72 $\mu V/\sqrt{Hz}$ (fig. 38). In particular, CMOS MUX white noise appears to be independent of clock frequency. Figure 39 shows the result of the "bandwidth-corrected" CMOS MUX white noise added in quadrature with the effective resistance Johnson noise for channel 22. For the several cases illustrated in figure 39, Johnson noise was negligible in comparison with the uncorrected CMOS MUX white noise. The Johnson noise bandwidth was 0.10 Hz.

Next, we would like to compare the MUX spot noise in the static mode (fig. 27) with that in the dynamic mode 3.2-kHz clock (fig. 29). The corrected spot-noise levels from 0.25 to 10 Hz for the two spectra are tabulated in table 4 and plotted in figure 39. Amplifier bandwidth was reduced to 80 Hz in both cases. The spot noise for both plots is identical at 3.0 Hz. For readout frequencies greater than 3.0 Hz, the spot noise for the static mode becomes less than that in the 3.2-kHz-clock case. In the dynamic mode, the fast Fourier transformation associated with correlated sampling suppressed the low-frequency $1/f$ or $1/\sqrt{f}$ components (ref. 18).

Noise Dependence on Temperature

The spectral noise density of the MUX did not vary significantly when the MUX was operating at different temperatures, namely, 4.9 K, 77 K, and 300 K. Figures 21 and 27 show that the noise spectra of the MUX operating in the static mode at 4.9 K and at 300 K are similar. We could not compare the noise spectra of the CMOS MUX operating in the dynamic mode at 4.9 K and at 300 K because the drive electronics might have been too noisy when the MUX noise was measured at 4.9 K (fig. 22).

The dynamic-mode noise levels of the MUX operating at 77 K and at 300 K are quite similar. For the same drain current of 0.79 μA (figs. 29 and 40), the bandwidth-corrected spot noise at 10 Hz is about 2.1 $\mu V/\sqrt{Hz}$ for 77 K and 3 $\mu V/\sqrt{Hz}$ for 300 K (see fig. 39). With the MUX operating at 400-μA drain current (figs. 31 and 41), the spot noise at 10 Hz is 100 $\mu V/\sqrt{Hz}$ or 6.72 $\mu V/\sqrt{Hz}$ after amplifier bandwidth correction (see fig. 38).

Notice that in the dynamic mode, the MUX spot noise at 10 Hz is higher for operation in the strong-inversion region than it is for operation in the weak-inversion region. The opposite effect was observed for the MUX operating in the static mode (see Static Noise in sec. 8).

9. CONCLUSIONS

Extensive measurements were made to evaluate the 32-channel CMOS MUX at room temperature and at 4.9 K. The CMOS MUX was operated in the static mode and in the dynamic mode. In the static mode, a selected channel of the CMOS MUX was made to turn on and remained on while other channels were turned off. In the dynamic mode, external clock pulses were required to drive the CMOS MUX at various clocking frequencies.

With the addition of a 10-kΩ source resistor, the FET channel gain of the input FET amplifier was measured and found to be 0.53 when operating at room temperature and 0.63 when operating at 4.9 K. The FET channel gain did not vary significantly with clock frequency when measured at different operating temperatures. The off-channel leakage current of the CMOS at 4.9 K was 0.23 pA/channel. Electrical crosstalk between adjacent channels was measured to be 0.55% at 4.9 K.

In the static mode, the spot noise at 10 Hz (7 $\mu V/\sqrt{Hz}$ or 0.45 $\mu V/\sqrt{Hz}$ if the amplifier bandwidth was reduced to 80 Hz) was about the same for both room temperature and 4.9-K operation. It was believed that for both cases, the input FET amplifier was operating near the weak-inversion region. In the dynamic mode, the spot noise at 10 Hz measured at room temperature was 100 $\mu V/\sqrt{Hz}$ (or 6.7 $\mu V/\sqrt{Hz}$ after reducing the amplifier bandwidth to 80 Hz), which was independent of drain currents (10 μA to 400 μA). The channel of the input FET amplifier was strongly inverted and was operating in the saturation region. Dynamic-mode noise results at 4.9 K were not reliable for comparison. The actual dynamic-mode noise level at 4.9 K may very likely be better than those presented in this report. We would expect the dynamic-mode noise levels at 4.9 K to be at least as low as the room temperature or 77-K case; actually, it is believed that it would be lower, if it were not limited by the noise in the test equipment or external electronics.

The measurements show that the 32-channel CMOS MUX can be made to operate at liquid-helium temperatures. Although the noise data for the 4.9-K operation are not validated and the voltage gain is slightly low, this device has low off-channel leakage currents and low electrical crosstalk. Additional noise data are required in order to assess the usefulness of the CMOS MUX for low-level signal processing. The spot noise at 10 Hz of the CMOS MUX operating at 4.9 K in the static mode is about 10 times higher than that measured by Arentz et al. (ref. 1) and Sclar (ref. 14) on a single-channel MOSFET. However, it is clear that the CMOS MUX can be used to process "housekeeping" data.

10. RECOMMENDATIONS

In order to advance our understanding of the 32-channel CMOS MUX operation, it is recommended that the following measurements should be made: (1) CMOS MUX dynamic-mode noise at 4.9 K, (2) clock-frequency limitation of the CMOS MUX, and (3) frequency response of the input FET amplifier. The dynamic-mode noise should be spot-checked to verify the bandwidth adjustment factor. Since on-focal-plane signal processing at low temperature requires low power dissipation from the devices, FETs operating in the weak-inversion region would certainly be preferred over those operating in the strong-inversion region. However, performance parameters should be investigated further before we can assess the advantages of operating in the weak-inversion region.

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TABLE 1.- DRIVE ELECTRONICS "CORRECTED" SPOT NOISE [from figs. 8-10]

Clock frequency, kHz	2.5	5	25
Amplifier bandwidth used in measurement, kHz	17	17	17
Uncorrected in-band rms noise (2.5 to 10 Hz), μV	197.18[a]	164.32	68.46
Reduced amplifier bandwidth (dc to sampling frequency) (f_s), Hz	62.5	125	625
Corrected in-band rms noise (2.5 to 10 Hz), μV	11.96[b]	14.09	13.13
Corrected spot noise at 2.5 to 10 Hz, $\mu V/\sqrt{Hz}$	4.37[c]	5.14	4.79

[a] (Uncorrected spot noise at 10 Hz) × $(10 - 2.5)^{1/2}$.

[b] Assume the new bandwidth to be dc to the sampling frequency, f_s. Then the uncorrected in-band rms noise is reduced by the factor, $(17\times10^3/f_s)^{1/2}$.

[c] Assuming the spot noise is flat from 2.5 to 10 Hz, then corrected spot noise = (corrected in-band rms noise)/$(10 - 2.5)^{1/2}$.

TABLE 2.- INPUT CIRCUIT JOHNSON NOISE

Parameter	Channel 21 (with detector)	Channel 22 (without detector)
R_{LOAD} (R_L), Ω	10^{10}	4.5×10^{11}
$R_{DETECTOR}$ (R_D), Ω		
300 K	75	1.1×10^{12} (Eltec Resistor)
77 K	300	1.1×10^{12} (Eltec Resistor)
4.9 K	10^{12}	1.1×10^{12} (Eltec Resistor)
$R_{EFFECTIVE}$, Ω		
300 K	75	3.17×10^{11}
77 K	300	3.17×10^{11}
4.9 K	10^{10}	3.17×10^{11}
FET input capacitance, C, pF	5	5
Noise Bandwidth, Δf, Hz		
300 K	4.2×10^{8}	0.10
77 K	1.1×10^{8}	0.10
4.9 K	3.18	0.10
Johnson noise, $\mu V/\sqrt{Hz}$		
300 K	1.1×10^{-3}	72.45
77 K	1.1×10^{-3}	36.70
4.9 K	1.64	9.26

TABLE 3.- CMOS MUX "CORRECTED" SPOT NOISE: DYNAMIC MODE

	Fig. 28	Fig. 28	Fig. 29	Fig. 29	Fig. 31	Fig. 32
Channel	21	21	22	22	21	21
Operating conditions	V_{gs} = -2.8 V I_{DS} = 0.14 μA T = 300 K	V_{gs} = -1.0 V I_{DS} = 0.14 μA T = 300 K	V_{gs} = -2.8 V I_{DS} = 0.7 μA T = 300 K	V_{gs} = -0.8 V I_{DS} = 0.7 μA T = 300 K	10 μA ≤ I_{DS} ≤ 400 μA T = 300 K	V_{gs} = -1.4 V T = 300 K
Clock frequency, Hz	3200	3200	3200	3200	3200	320
Amplifier BW, Hz	19,400	19,400	19,400	19,400	17,700	19,400
Uncorrected spot noise, $\mu V/\sqrt{Hz}$ [a]	45 (2.5 to 10 Hz)	18 (2.5 to 10 Hz)	29.5 (2.5 to 10 Hz)	45 (2.5 to 10 Hz)	100 (2.5 to 10 Hz)	180 (0.25 to 2 Hz)
Uncorrected in-band rms noise, μV	123.24	49.30	80.79	123.24	273.86	238.12
New amplifier BW cutoff, f_s, Hz	80	80	80	80	80	8
Corrected in-band rms noise, μV	7.914	3.17	5.188	7.914	18.41	4.84
Corrected spot noise, $\mu V/\sqrt{Hz}$ [a]	2.89 (2.5 to 10 Hz)	1.166 (2.5 to 10 Hz)	1.89 (2.5 to 10 Hz)	2.89 (2.5 to 10 Hz)	6.72 (2.5 to 10 Hz)	3.66 (0.25 to 2 Hz)

	Fig. 33	Fig. 34	Fig. 35	Fig. 40	Fig. 41
Channel	22	21	22	22	21
Operating conditions	V_{gs} = -1.0 V T = 300 K	V_{gs} = -1.0 V T = 300 K	V_{gs} = -1.0 V T = 300 K	V_{gs} = -1.8 V I_{DS} = 0.79 μA T = 77 K	I_{DS} = 400 μA T = 77 K
Clock frequency, Hz	320	32	32	3200	3200
Amplifier BW, Hz	19,400	19,400	19,400	19,400	17,700
Uncorrected spot noise, $\mu V/\sqrt{Hz}$ [a]	130 (0.25 to 2 Hz)	600 (0.03 to 0.2 Hz)	425 (0.03 to 0.2 Hz)	32 (2.5 to 10 Hz)	100 (2.5 to 10 Hz)
Uncorrected in-band rms noise, μV	171.97	247.39	175.23	87.64	273.86
New amplifier BW cutoff, f_s, Hz	8	0.8	0.8	80	80
Corrected in-band rms noise, μV	3.49	1.59	1.125	5.63	18.41
Corrected spot noise, $\mu V/\sqrt{Hz}$ [a]	2.64 (0.25 to 2 Hz)	3.85 (0.03 to 0.2 Hz)	2.73 (0.03 to 0.2 Hz)	2.05 (2.5 to 10 Hz)	6.72 (2.5 to 10 Hz)

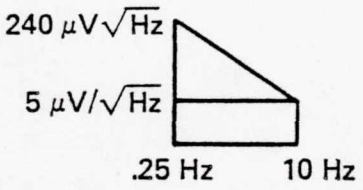
[a] Readout frequency range in parentheses.

TABLE 4.- CMOS MUX "CORRECTED" SPOT NOISE AT ROOM TEMPERATURE: STATIC VERSUS DYNAMIC [V_{gs} = -2.8 V, I_{DS} = 0.79 μA]

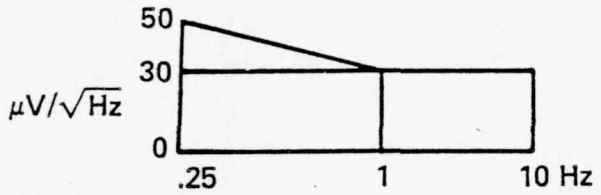
	Static (fig. 27)	Dynamic, 3.2 kHz (fig. 29)
Amplifier bandwidth, kHz	10	19.4
Reduced BW cutoff, Hz	80	80
Uncorrected in-band rms noise (0.25 → 10 Hz), μV	382.50[a]	124.64[b]
Reduction factor[c]	0.0894	0.0642
Corrected in-band[d] rms noise (0.25 → 10 Hz), μV	34.21	8.00
Corrected spot noise,[e] $\mu V/\sqrt{Hz}$		
0.25 Hz	21.47	3.275
0.5 Hz	8.586	2.569
1 Hz	4.472	1.926
3 Hz	1.789	1.798
5 Hz	0.876	1.862
6 Hz	0.751	1.991
8 Hz	0.59	1.862
10 Hz	0.447	1.734

NOTE

ⓐ STATIC



ⓑ DYNAMIC



ⓒ [(REDUCED BW CUTOFF)/(BW USED)]$^{1/2}$

ⓓ (REDUCTION FACTOR) x (UNCORRECTED IN-BAND RMS NOISE)

ⓔ (REDUCTION FACTOR) x (UNCORRECTED SPOT NOISE)

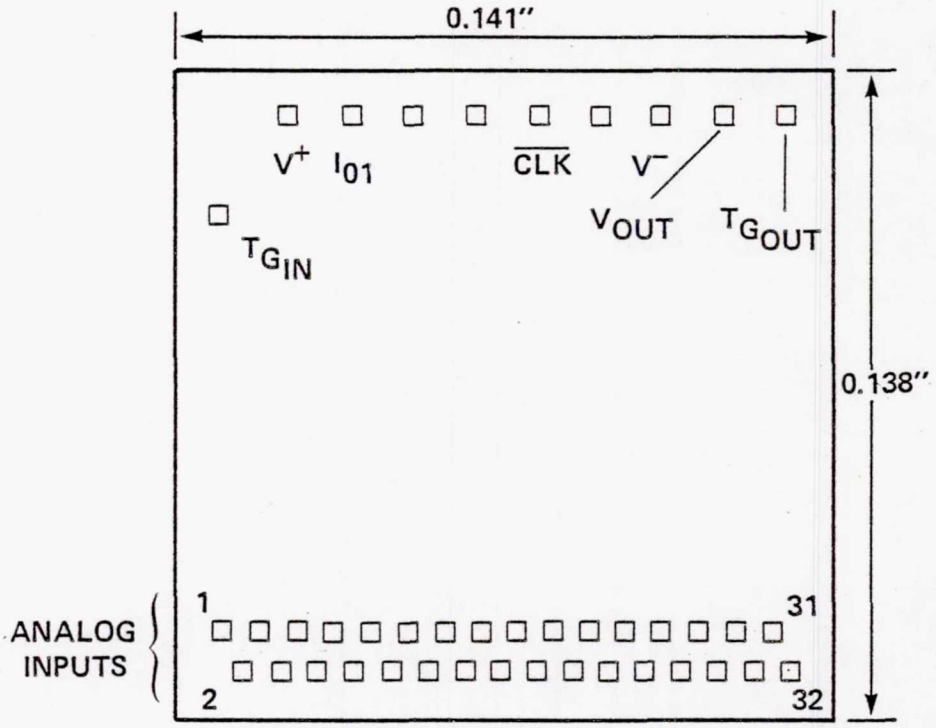


Figure 1.- CMOS MUX chip layout.

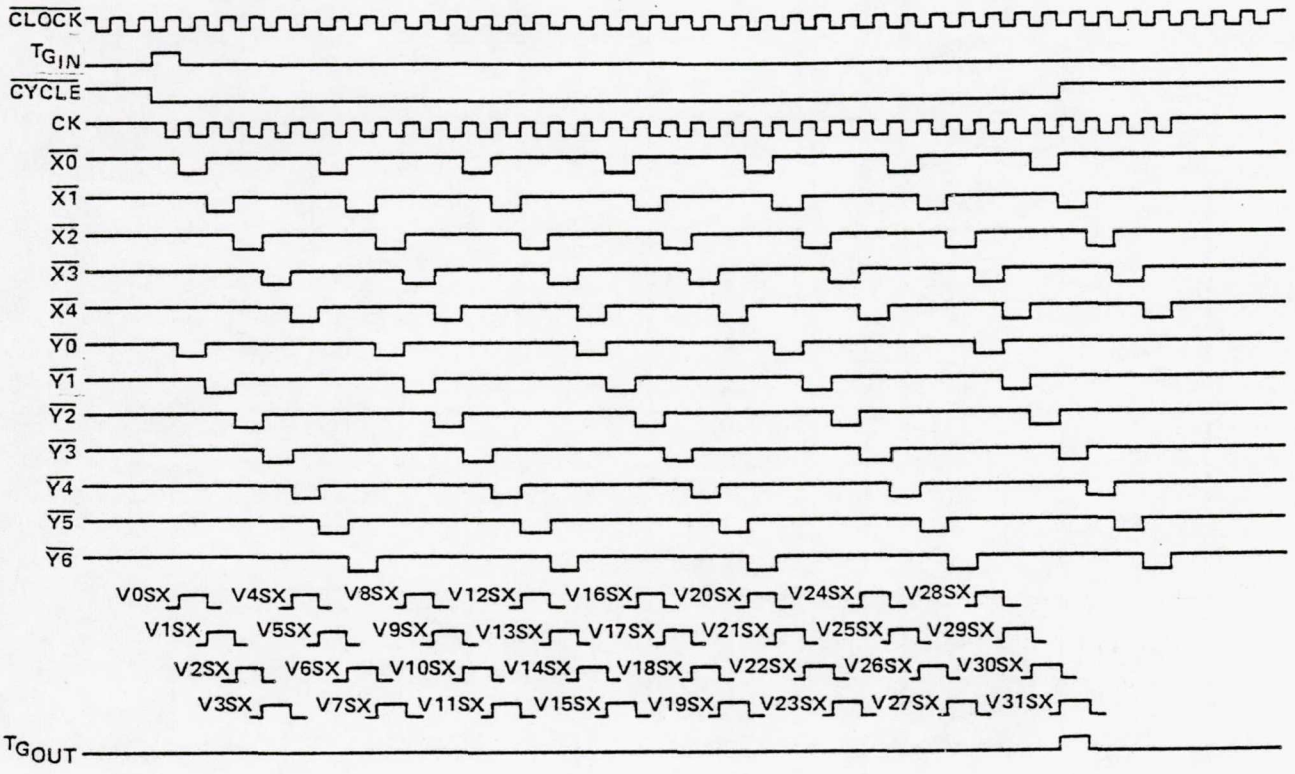


Figure 2.- CMOS timing diagram.

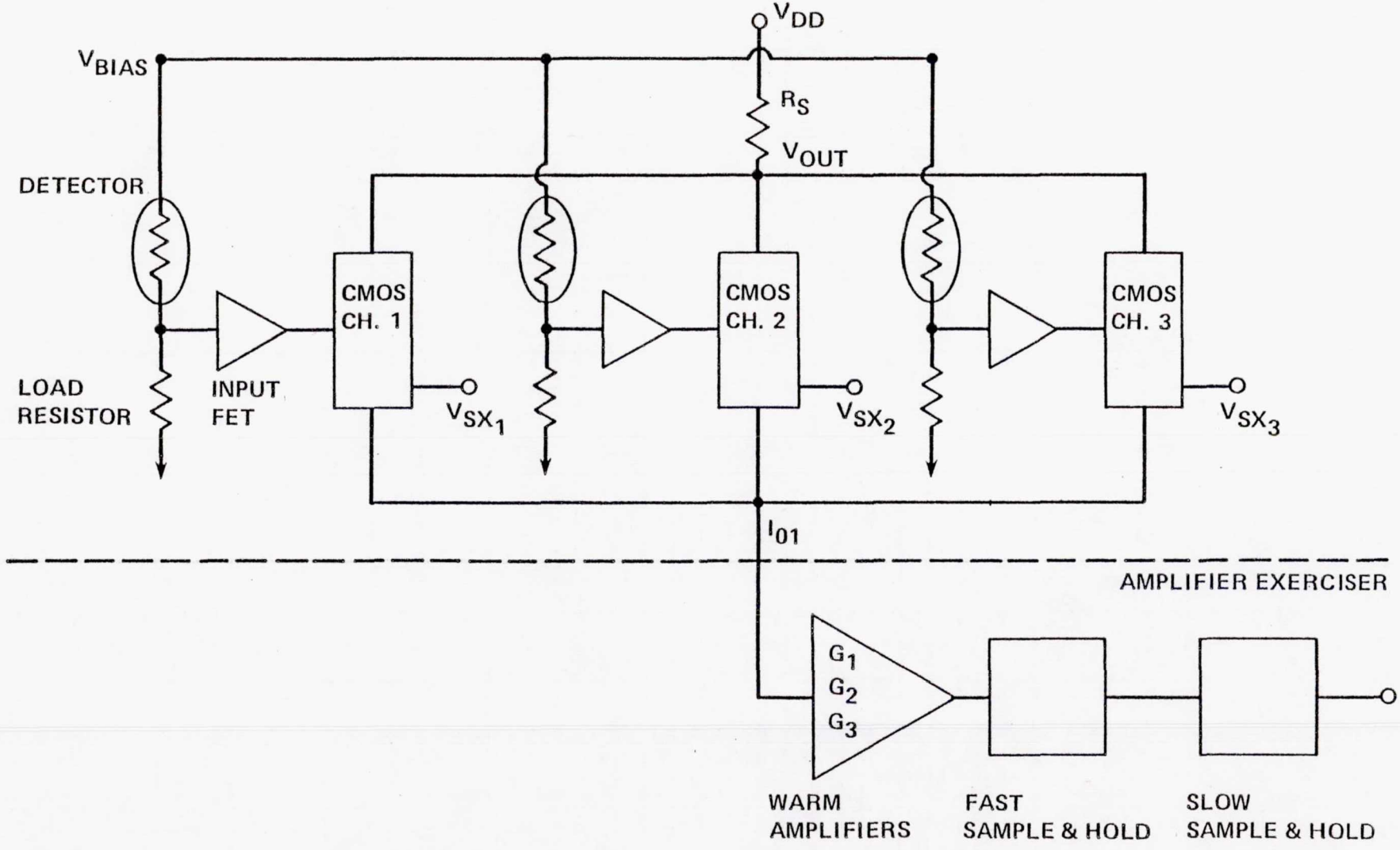


Figure 3.- CMOS multiplexer (3 of 32 channels).

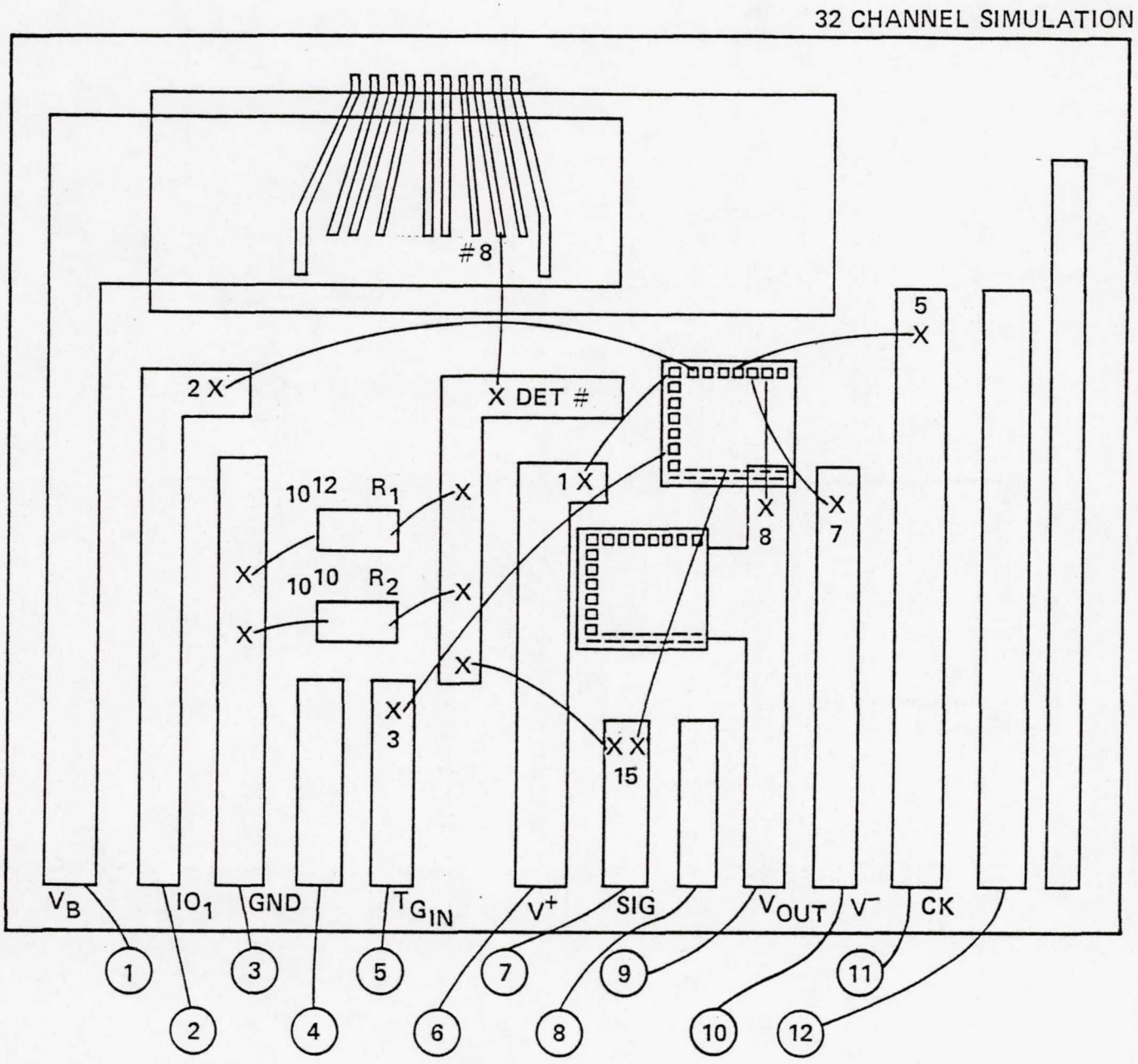


Figure 4.- Si-Ga infrared detector assembly.

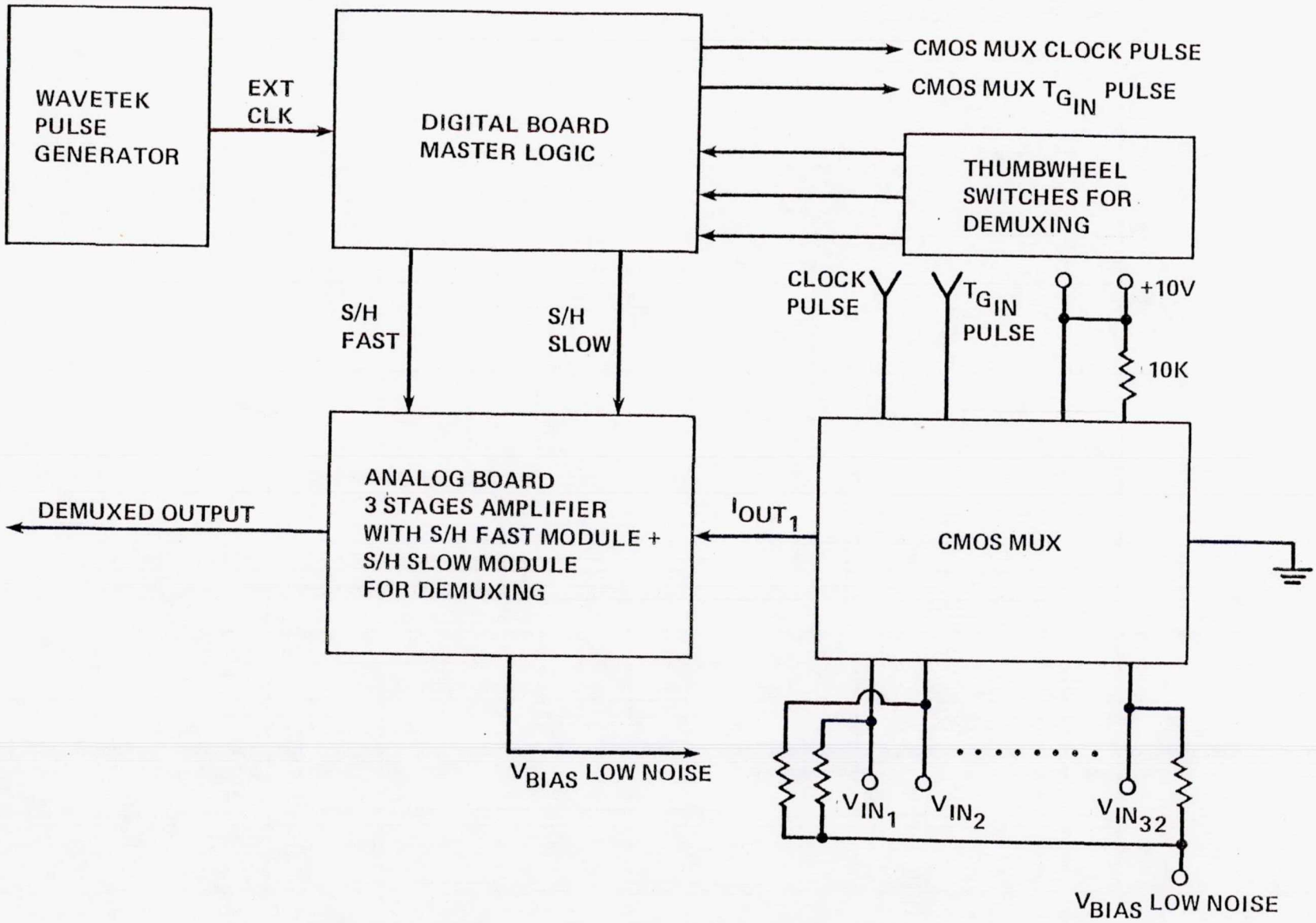


Figure 5.- Block diagram of CMOS multiplexer exerciser.

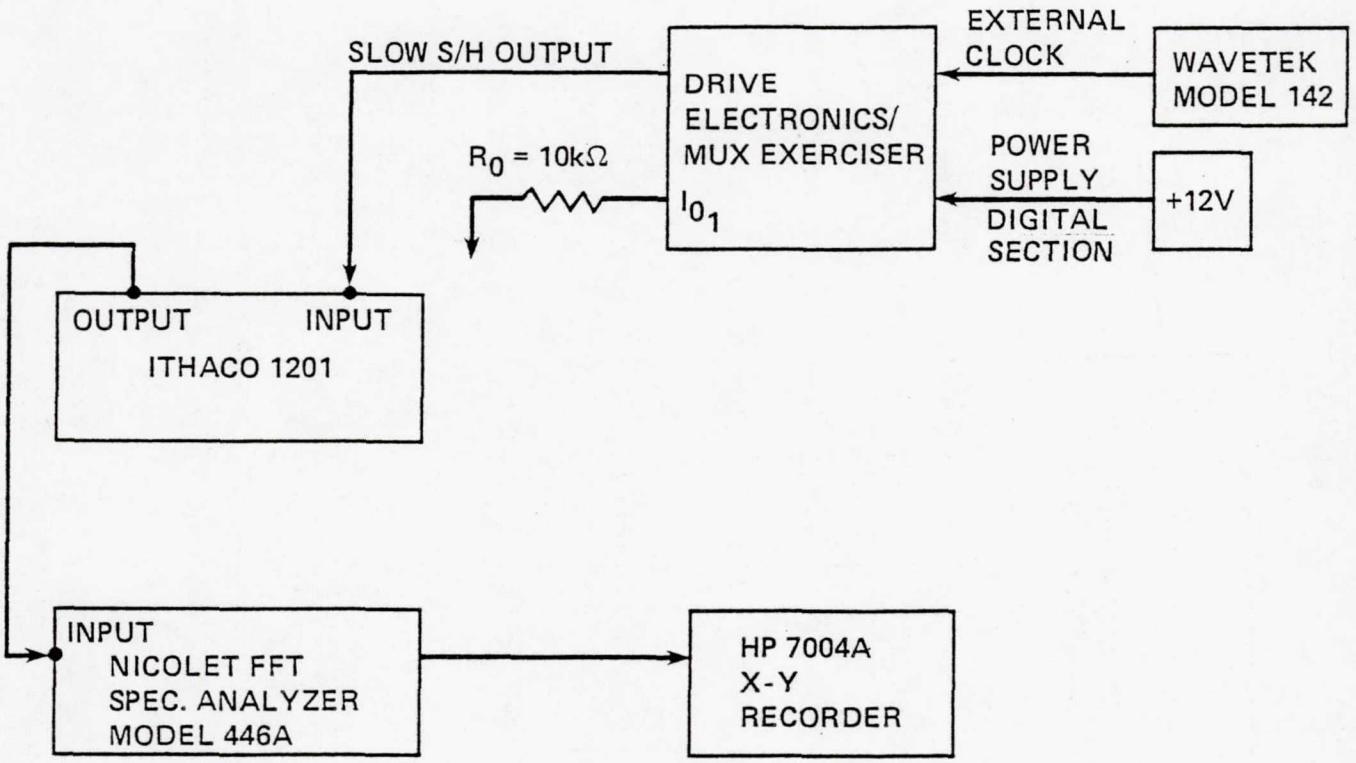


Figure 6.- Drive electronics noise measurement setup.

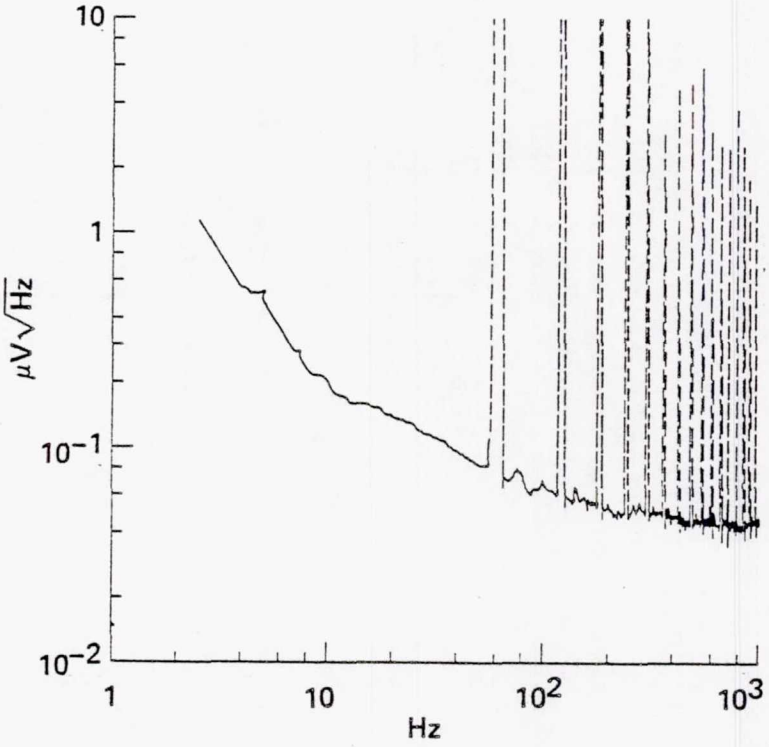


Figure 7.- MUX exerciser noise (static): BW_{amp} = 17.7 kHz; G_1 = 5, G_2 = 10, G_3 = 10.

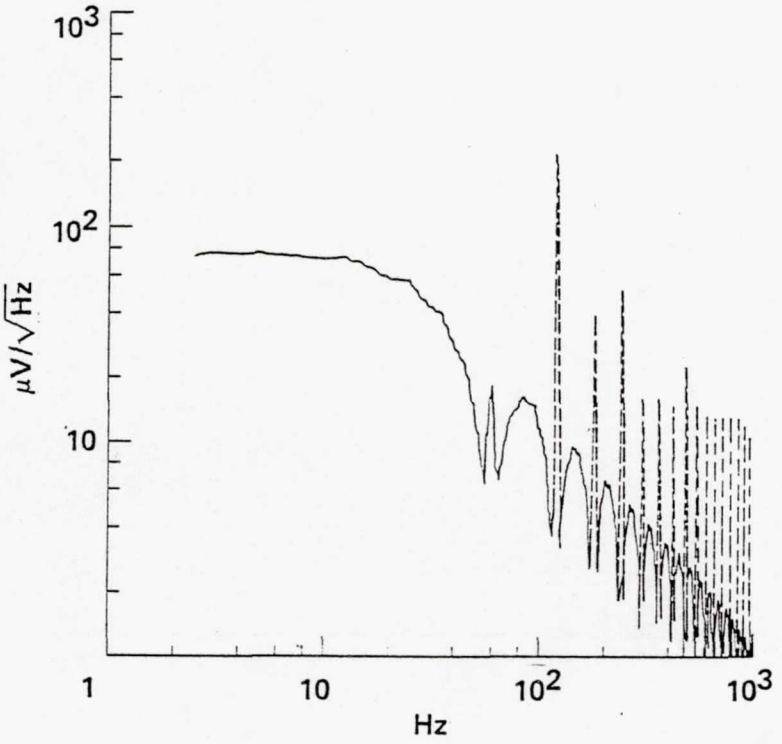


Figure 8.- MUX exerciser noise: 2.5 kHz clock; BW_{amp} = 17.7 kHz; G_1 = 5, G_2 = 1, G_3 = 1.

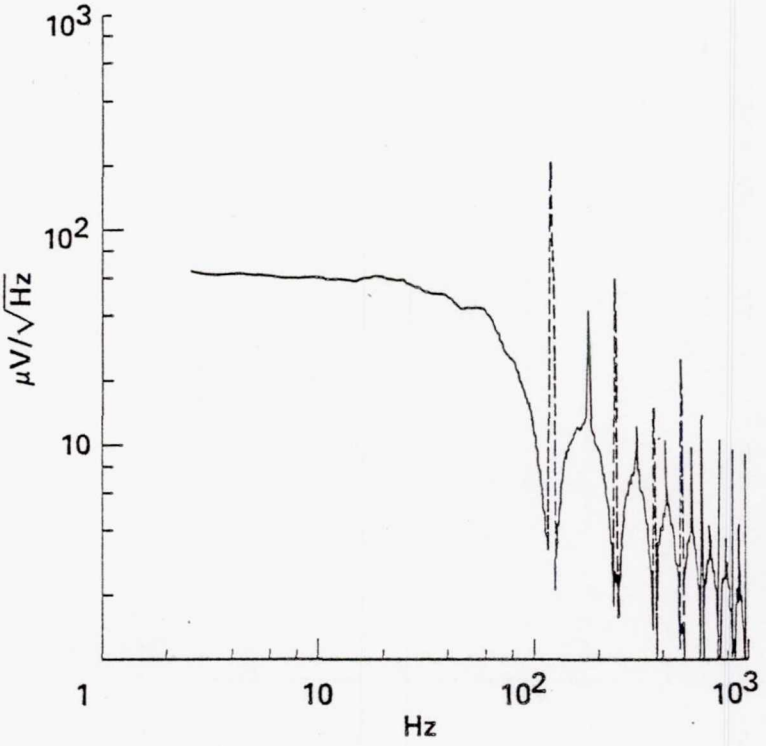


Figure 9.- MUX exerciser noise: 5 kHz clock; BW_{amp} = 17.7 kHz; G_1 = 5, G_2 = 1, G_3 = 1.

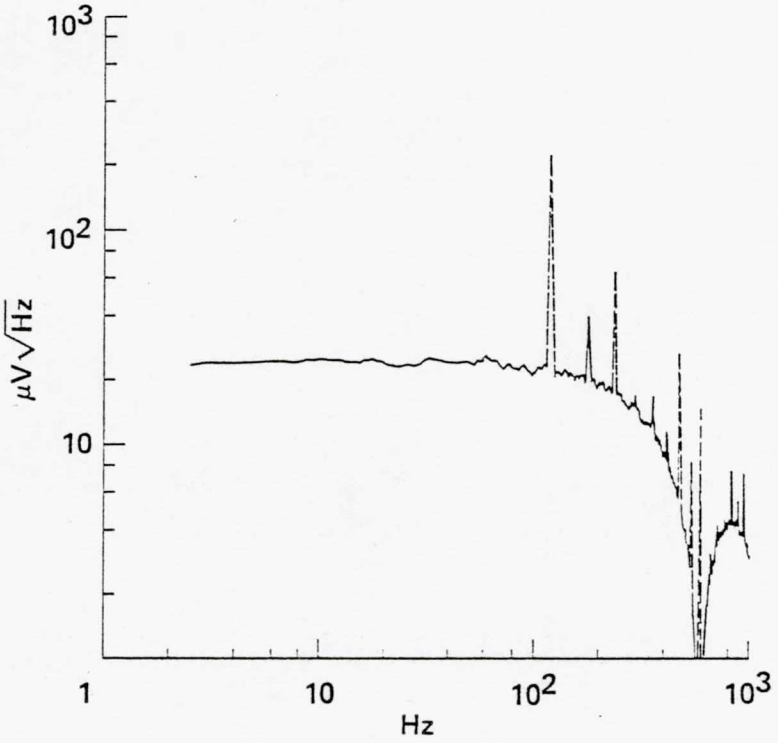


Figure 10.- MUX exerciser noise: 25 kHz clock; BW_{amp} = 17.7 kHz; G_1 = 5, G_2 = 1, G_3 = 1.

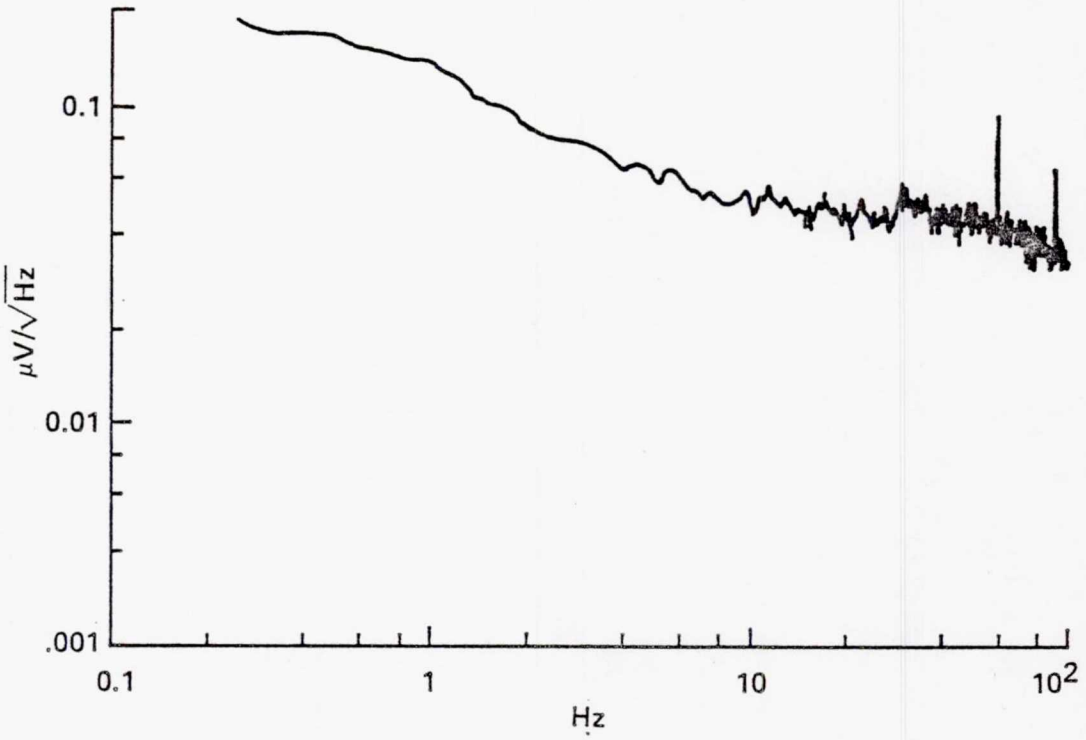


Figure 11.- MUX exerciser noise (static): BW_{amp} = 17.7 Hz; G_1 = 100, G_2 = 10, G_3 = 10.

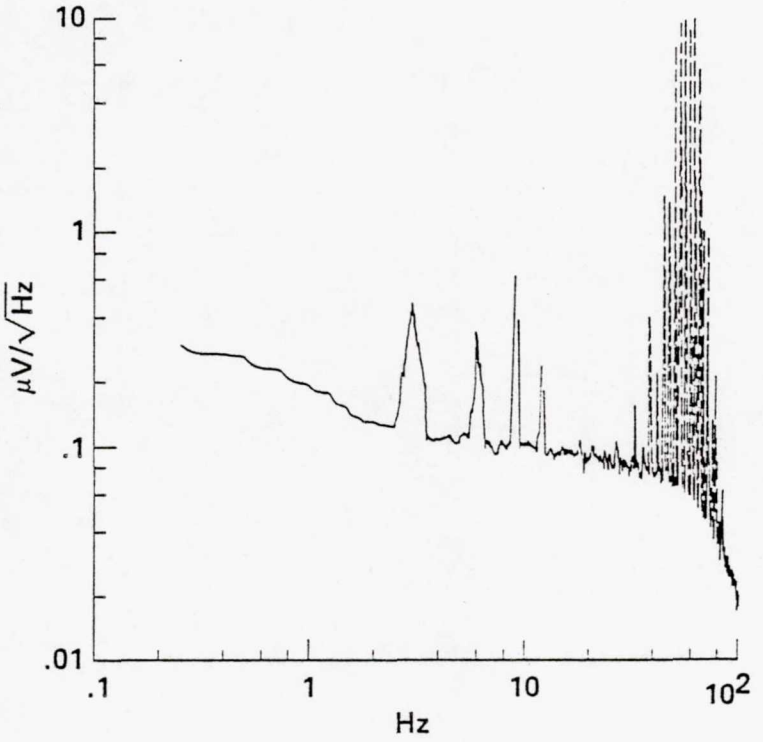


Figure 12.- MUX exerciser noise: 4.8 kHz clock; BW_{amp} = 17.7 kHz; G_1 = 100, G_2 = 10, G_3 = 10.

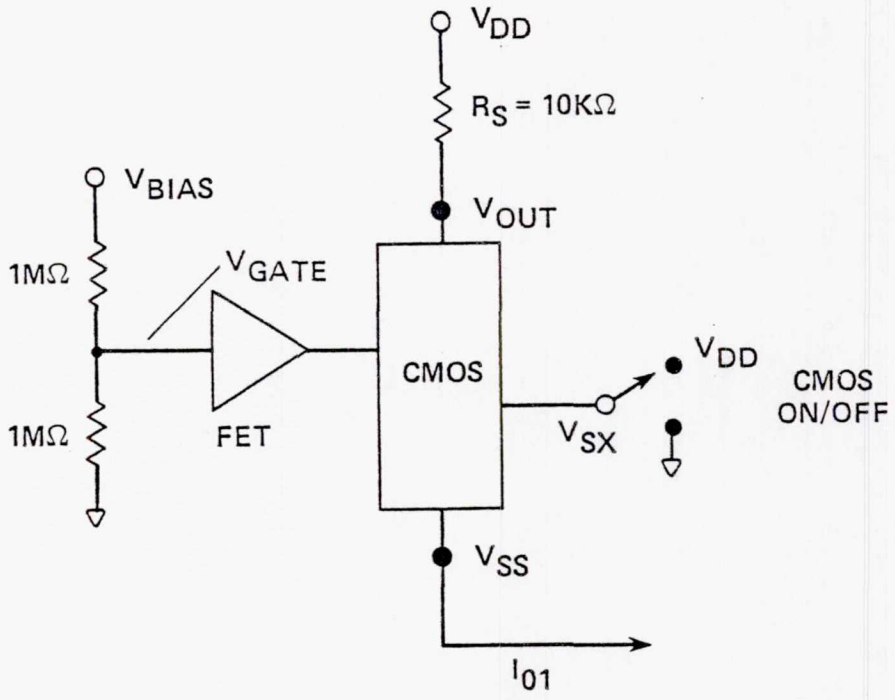


Figure 13.- Commercial CMOS breadboard test setup.

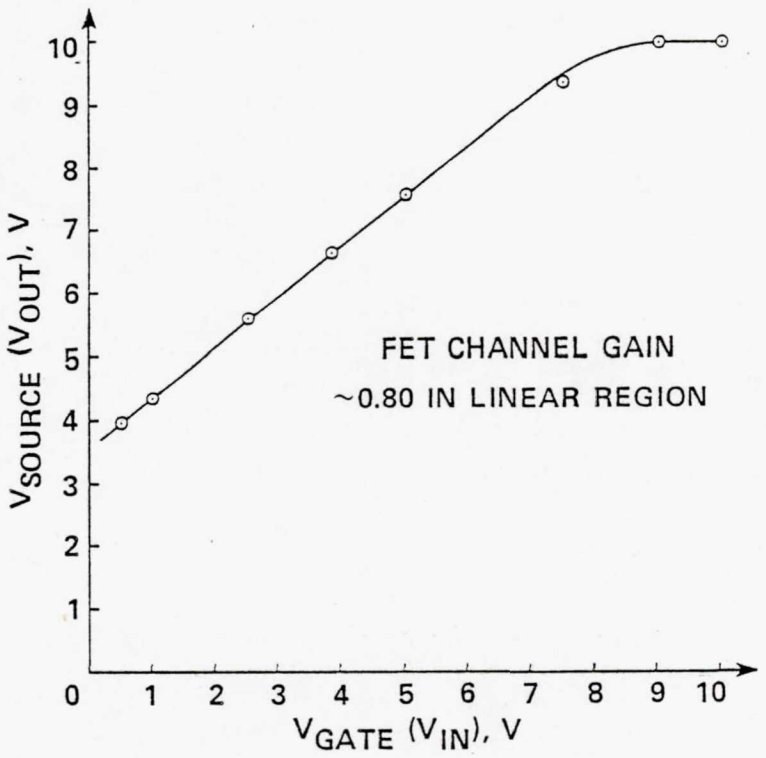


Figure 14.- Single-channel commercial CMOS, static mode output — gate voltage characteristics: R_{source} = 10 kΩ; room temperature.

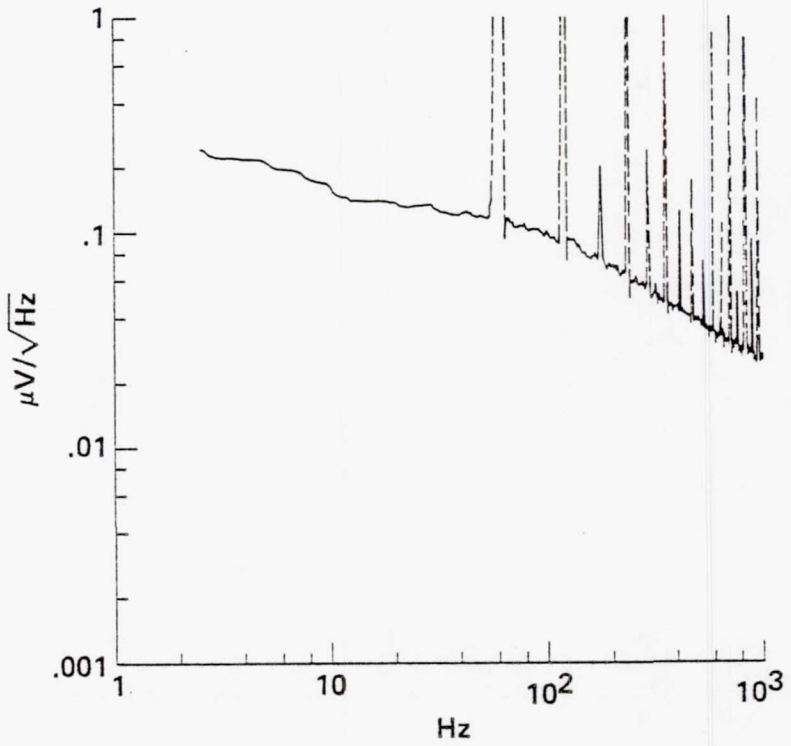


Figure 15.- Single-channel commercial CMOS noise, V_{in} = 3.84 V; I_{DS} = 280 μA; CMOS on; R_{ext} = 10 kΩ; BW_{amp} = 10 kHz.

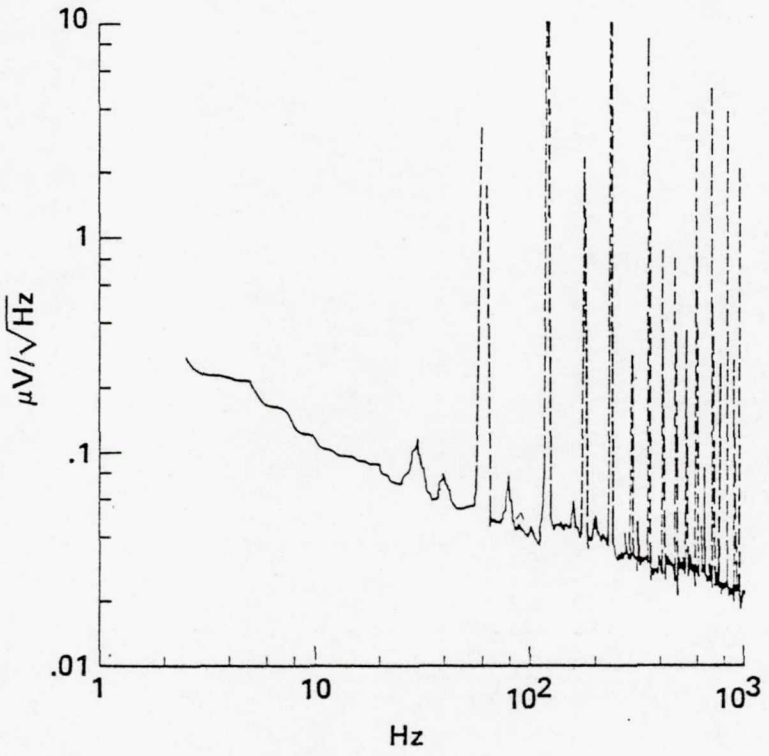
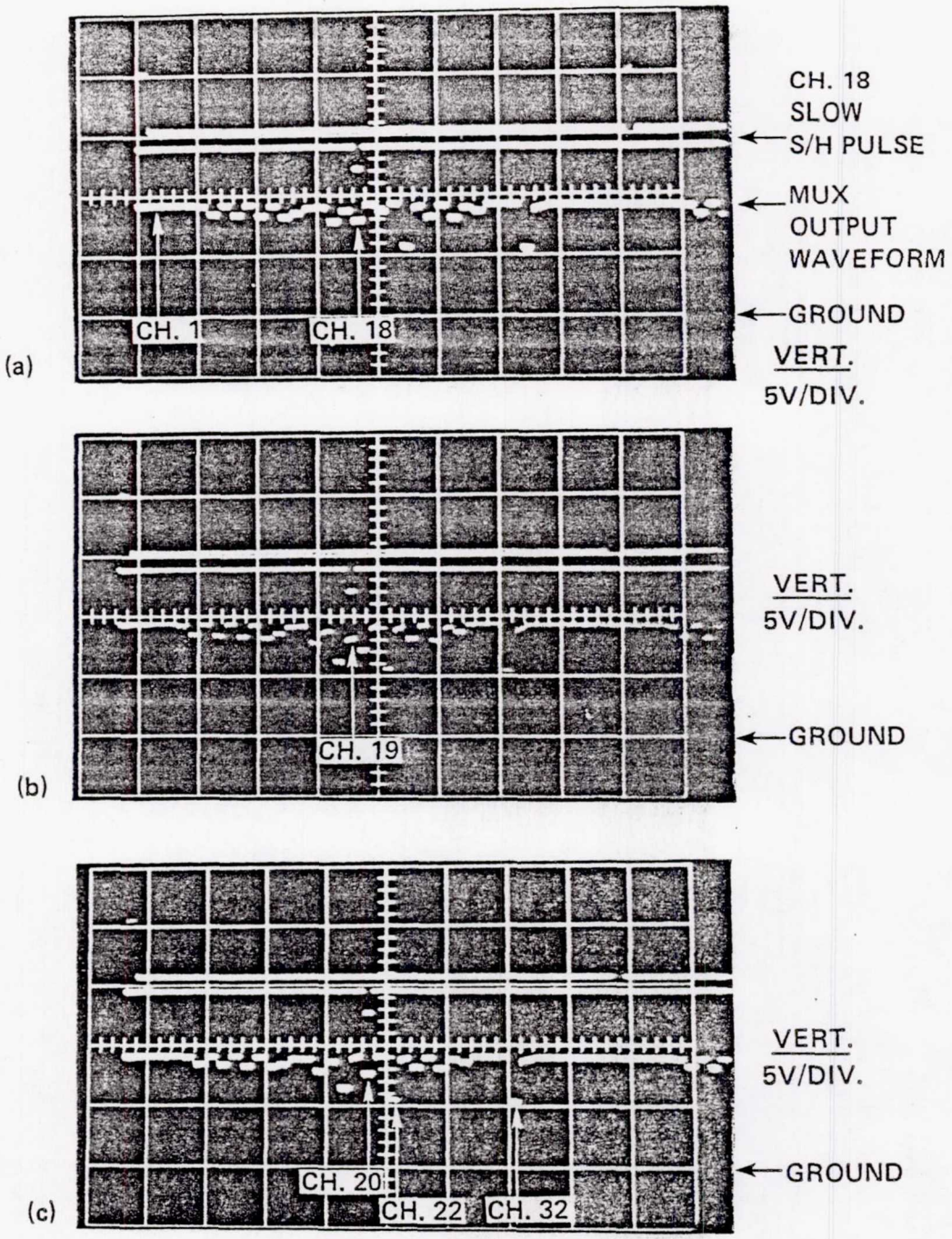


Figure 16.- Single channel commercial CMOS noise, V_{in} = 3.84 V: CMOS off; R_{ext} = 10 kΩ; BW_{amp} = 10 kHz.

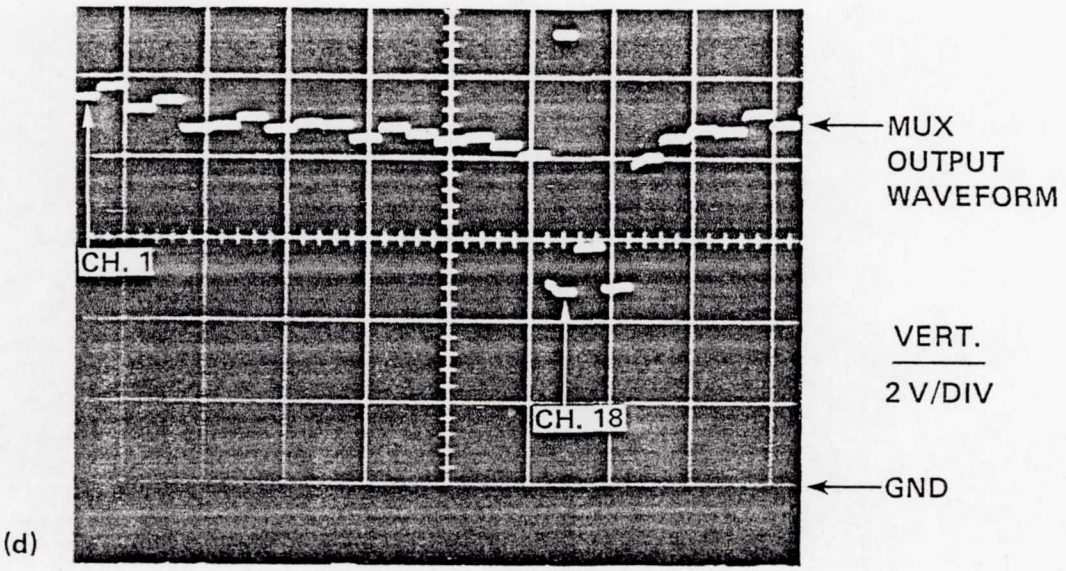


(a) Channel 18 (no detector), T = 300 K (10/22/80): Clock rate = 5 kHz, R_S = 10 kΩ, V_{gate} = 3.84 V, I_D = 255 μA.

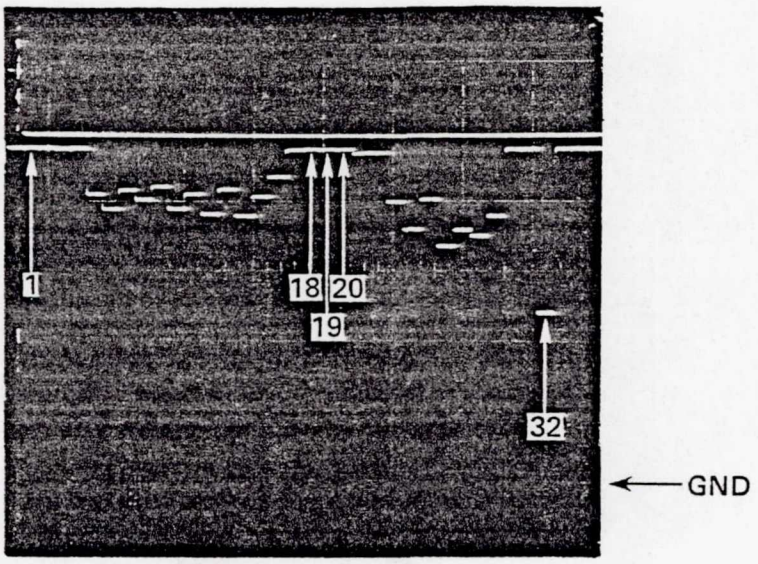
(b) Channel 19 (with detector), T = 300 K (10/22/80): Clock rate = 5 kHz, R_S = 10 kΩ, V_{gate} = 3.84 V, I_D = 215 μA.

(c) Channel 20 (no detector), T = 300 K (10/22/80): Clock rate = 5 kHz, R_S = 10 kΩ, V_{gate} = 3.84 V, I_D = 263 μA.

Figure 17.- CMOS multiplexer output waveform.



(d)

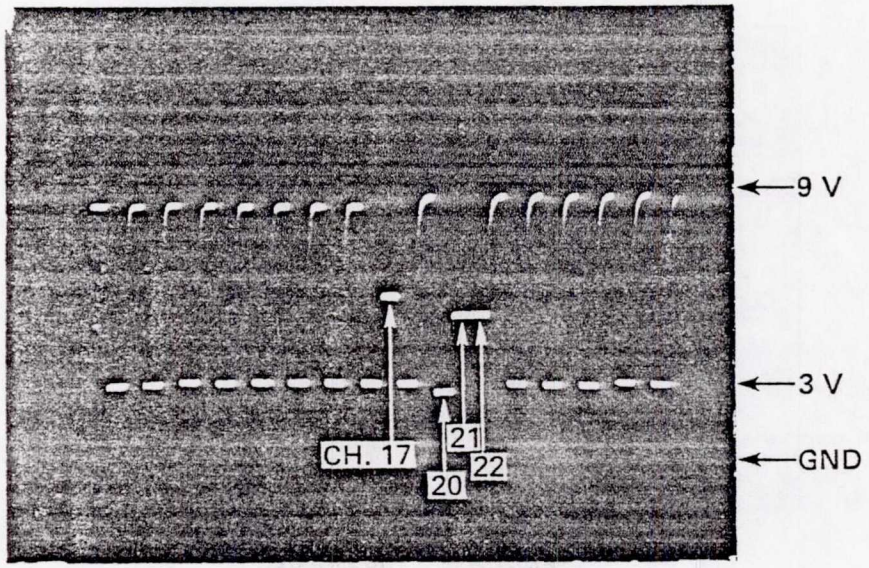


(e)

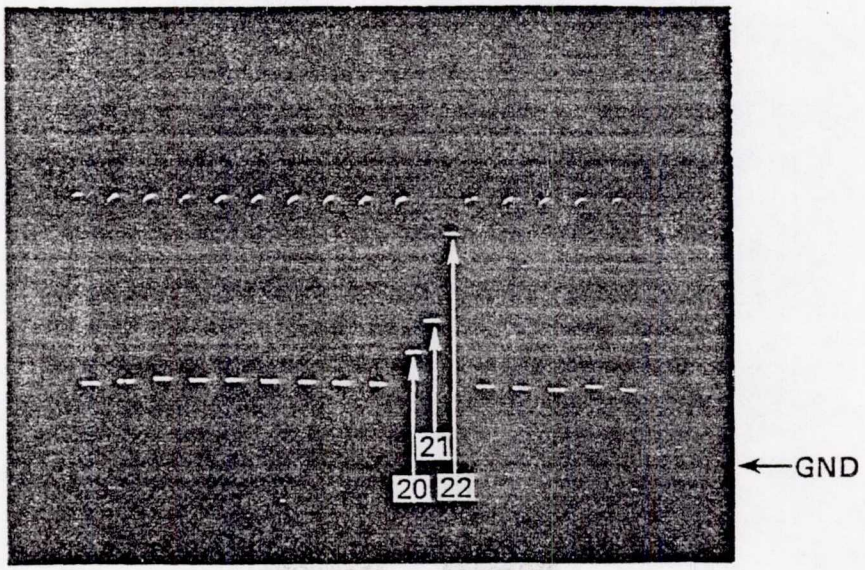
(d) Channels 18, 19, 20, T = 4.9 K (11/6/80): Clock rate = 5 kHz, R_s = 10 kΩ, V_{bias} = 10 V or V_{gate} = 0.25 V (Channels 18 and 20), V_{gate} = 1.5 V (Channel 19).

(e) Channels 18, 19, 20, T = 300 K (5/27/81): Clock rate = 4.8 kHz, R_s = 10 kΩ, V_{bias} = 10 V or V_{gate} = 10 V (Channels 18, 19, 20).

Figure 17.- Continued.



(f)



(g)

(f) Channels 20, 21, 22, T = 300 K (6/22/81): Clock rate = 3.2 kHz, R_s = 100 kΩ, V_{gate} = 1.1 V (Channel 20), V_{gate} = 3 V (Channels 21 and 22), V_{gate} = 10 V (odd inactive channels), V_{gate} = 0 V (even inactive channels).

(g) Channels 20, 21, 22, T = 77 K (8/14/81): Clock rate = 3.2 kHz, R_s = 100 kΩ, V_{bias} = 6.2 V, V_{out} = 3.8 V (Channel 20), V_{out} = 4.9 V (Channel 21), V_{out} = 7.8 V (Channel 22).

Figure 17.- Concluded.

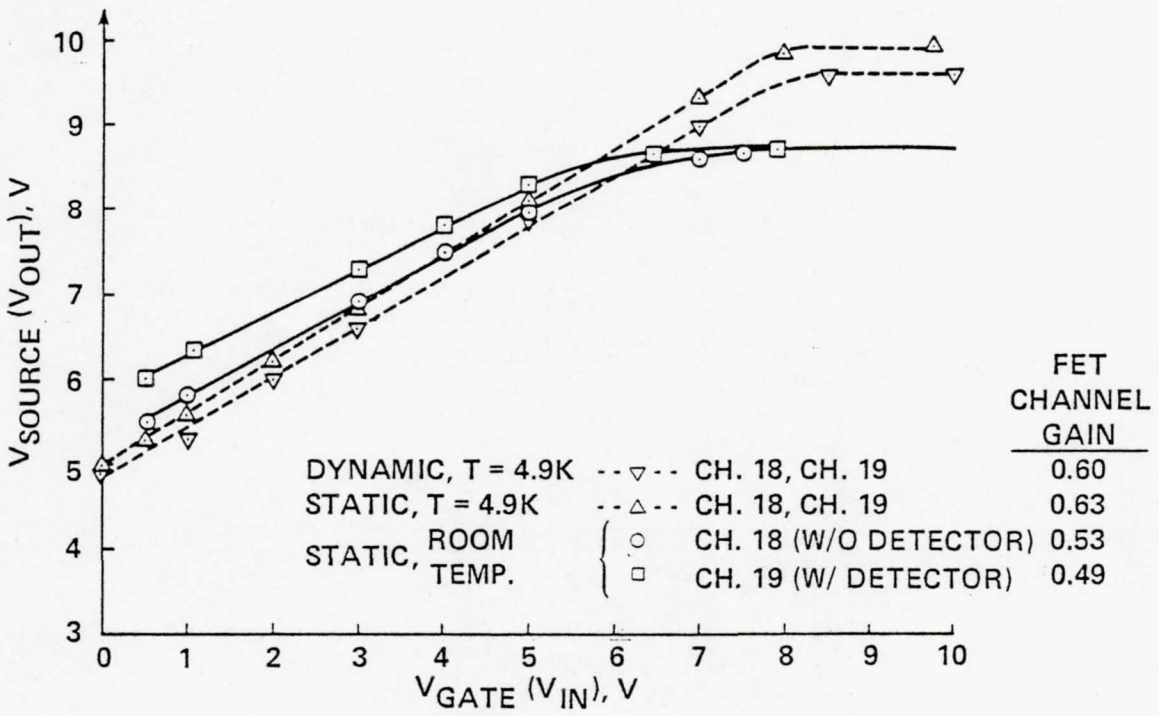


Figure 18.- Static and dynamic mode output-input FET gate voltage characteristics: at room temperature and 4.9 K for R_{source} = 10 kΩ.

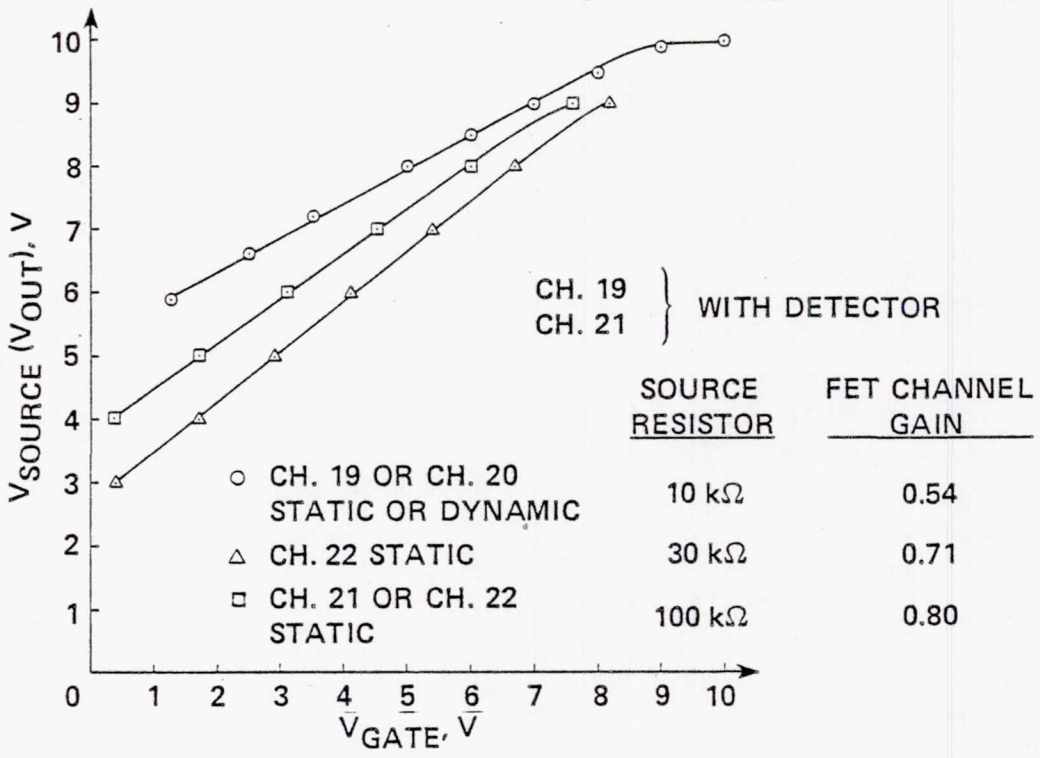


Figure 19.- Static and dynamic mode output-input FET gate voltage characteristics: at room temperature for R_{source} = 10, 30, and 100 kΩ.

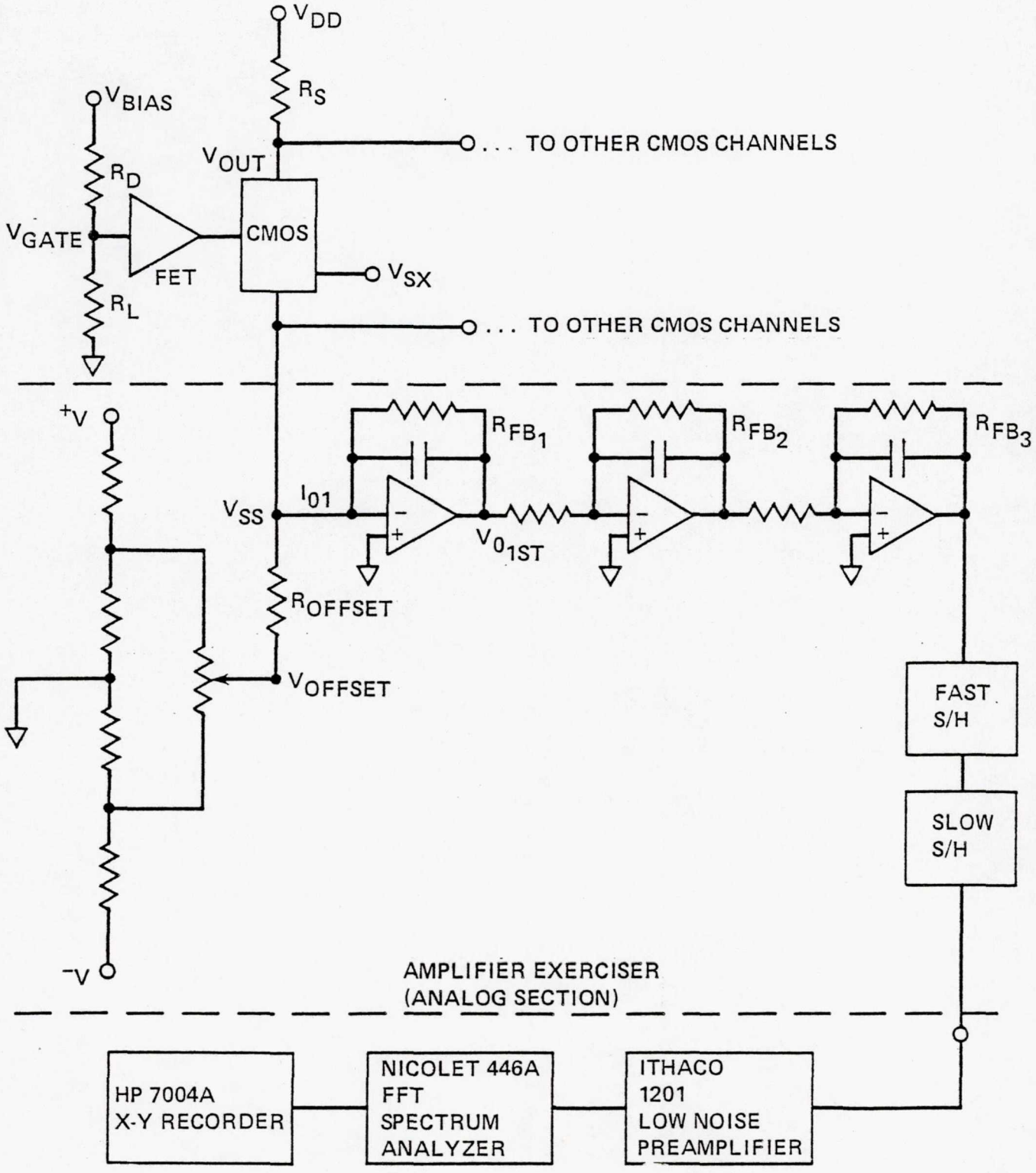
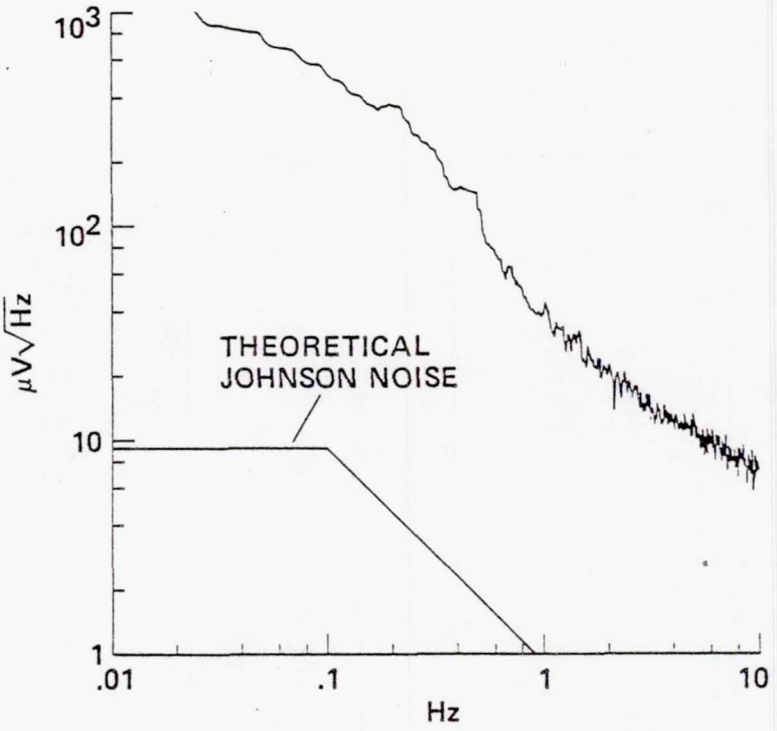
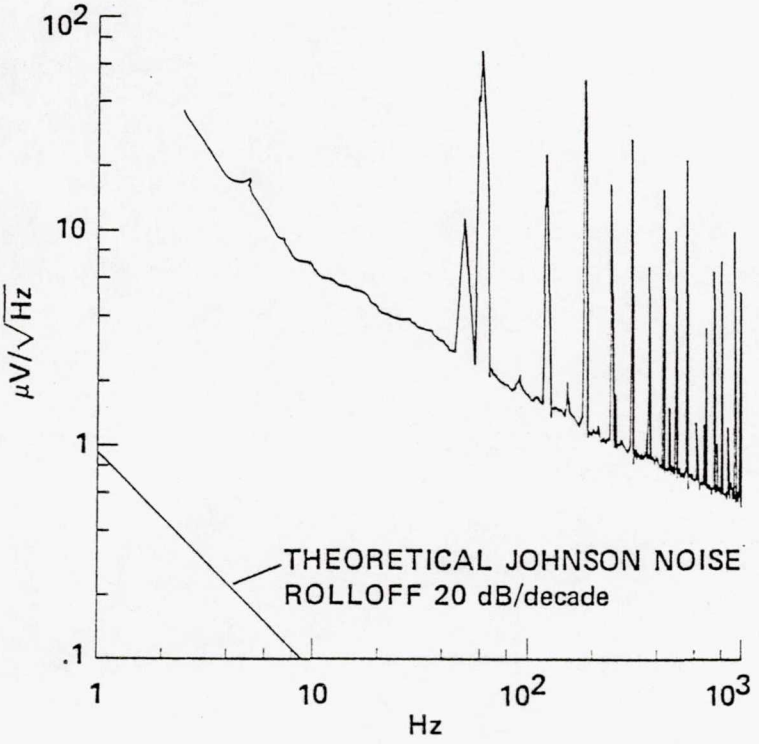


Figure 20.- CMOS multiplexer noise measurement setup, dynamic mode (only 1 channel shown).



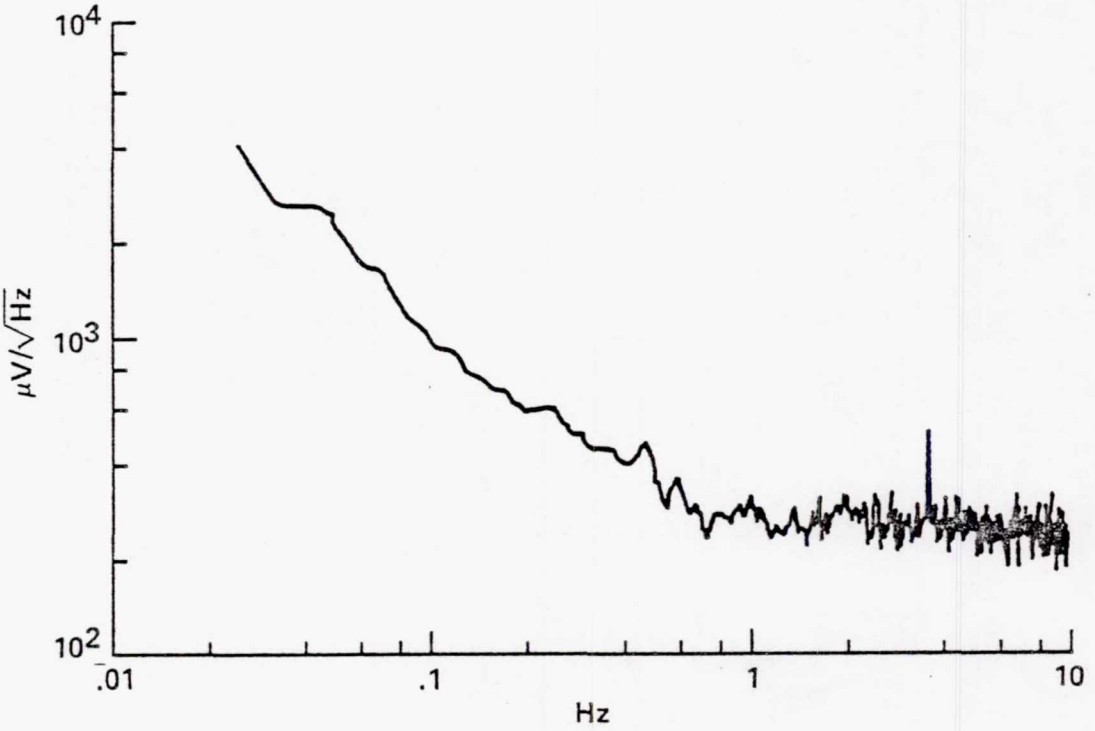
(a) Frequency range: 0.025 to 10 Hz.

Figure 21.- CMOS MUX noise (static) — Channel 18: T = 4.9 K, V_{gate} = 3.0 V, I_{DS} = 14 μA, BW_{amp} = 10 kHz.



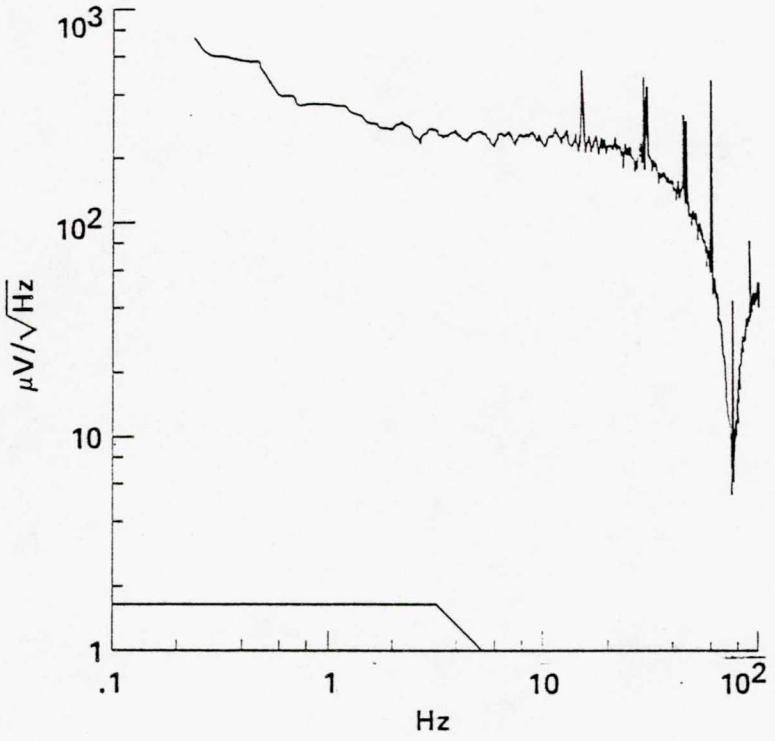
(b) Frequency range: 2.5 to 1000 Hz.

Figure 21.- Concluded.



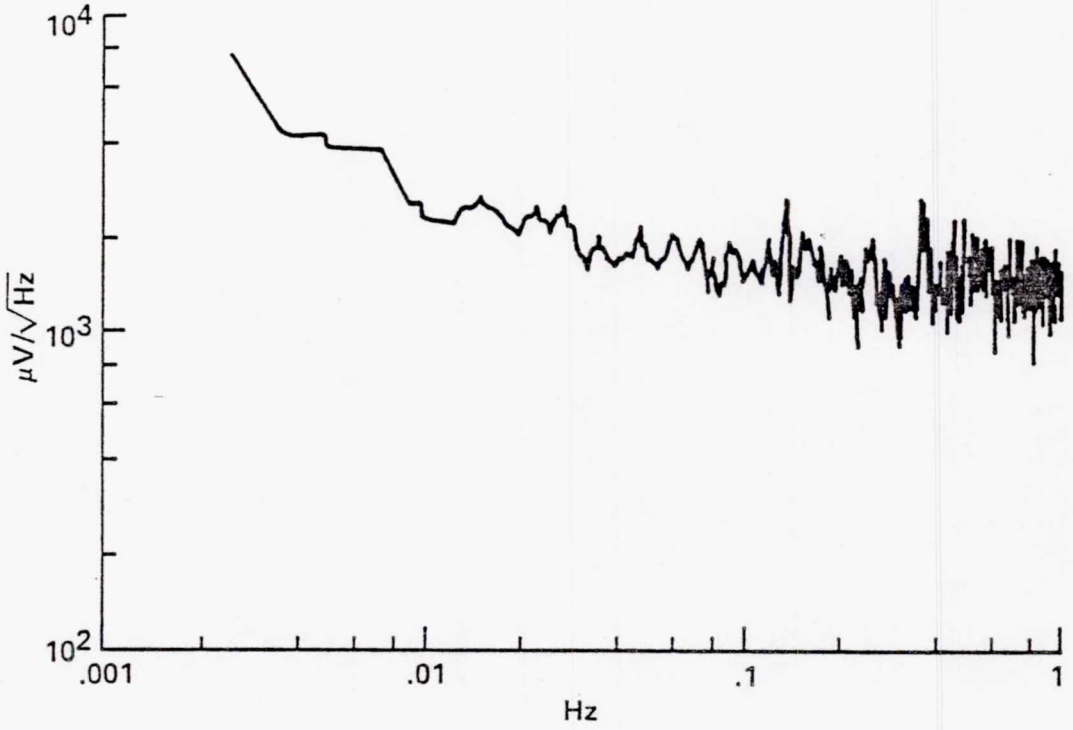
(a) Frequency range: 0.025 to 10 Hz.

Figure 22.- CMOS MUX noise (clock rate = 3.2 kHz) — Channel 18: T = 4.9 K, V_{gate} = 3.0 V, BW_{amp} = 17.7 kHz.



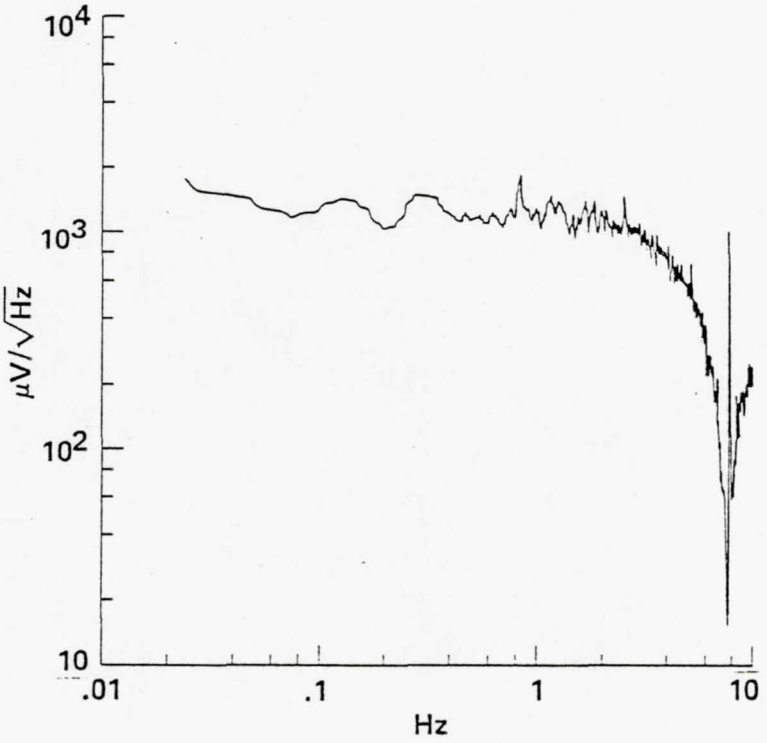
(b) Frequency range: 0.25 to 100 Hz.

Figure 22.- Concluded.



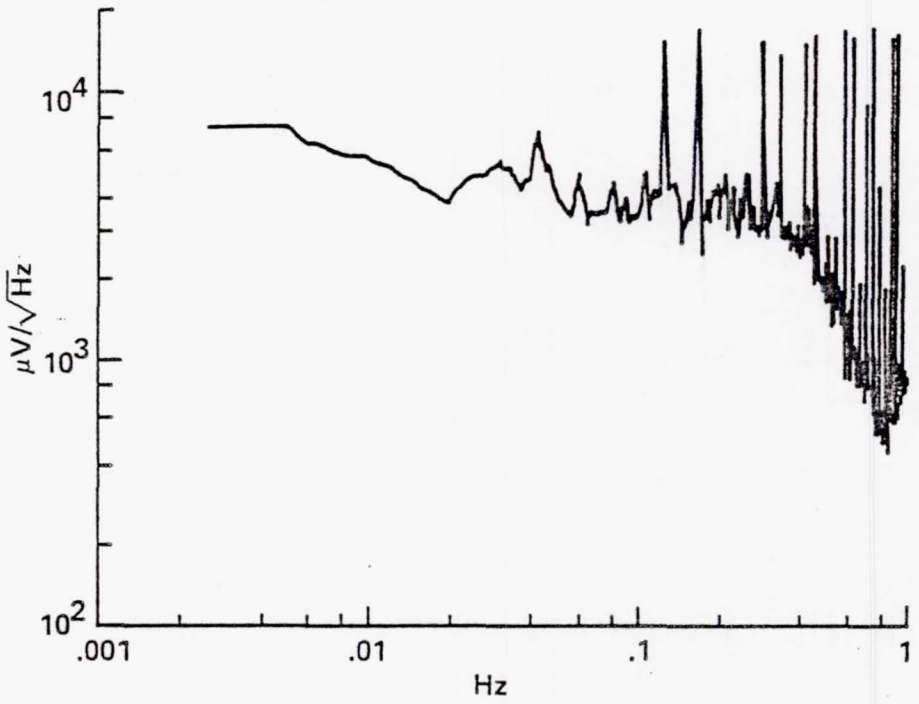
(a) Frequency range: 0.0025 to 1 Hz.

Figure 23.- CMOS MUX noise (clock rate = 320 Hz) — Channel 18: T = 4.9 K, V_{gate} = 3.0 V, BW_{amp} = 17.7 kHz.



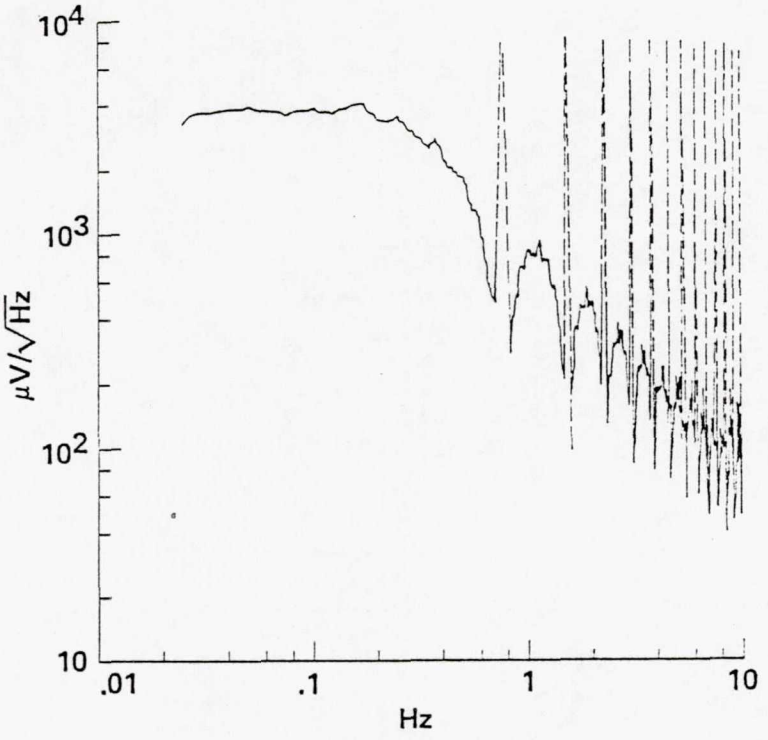
(b) Frequency range: 0.025 to 10 Hz.

Figure 23.- Concluded.



(a) Frequency range: 0.0025 to 1 Hz.

Figure 24.- CMOS MUX noise (clock rate = 32 Hz) — Channel 18: T = 4.9 K, V_{gate} = 3.0 V. BW_{amp} = 17.7 kHz.



(b) Frequency range: 0.025 to 10 Hz.

Figure 24.- Concluded.

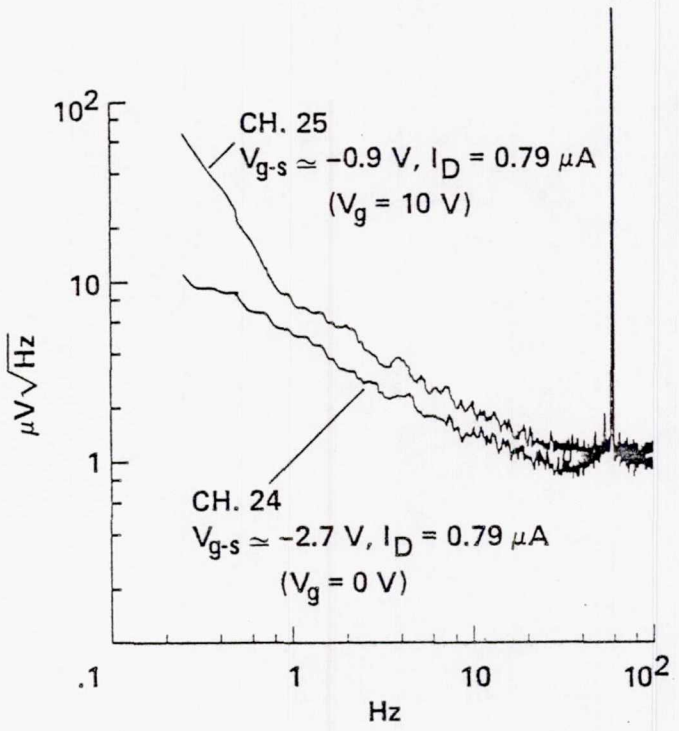


Figure 25.- CMOS MUX noise (static) — inactive channels: room temperature, BW_{amp} = 10 kHz.

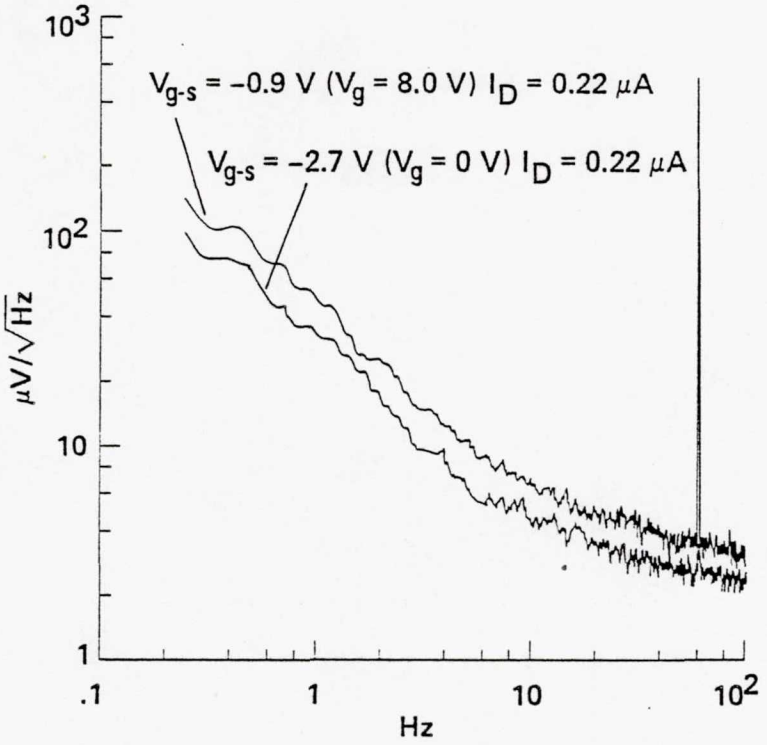


Figure 26.- CMOS MUX noise (static) — Channel 21: room temperature, BW_{amp} = 10 kHz.

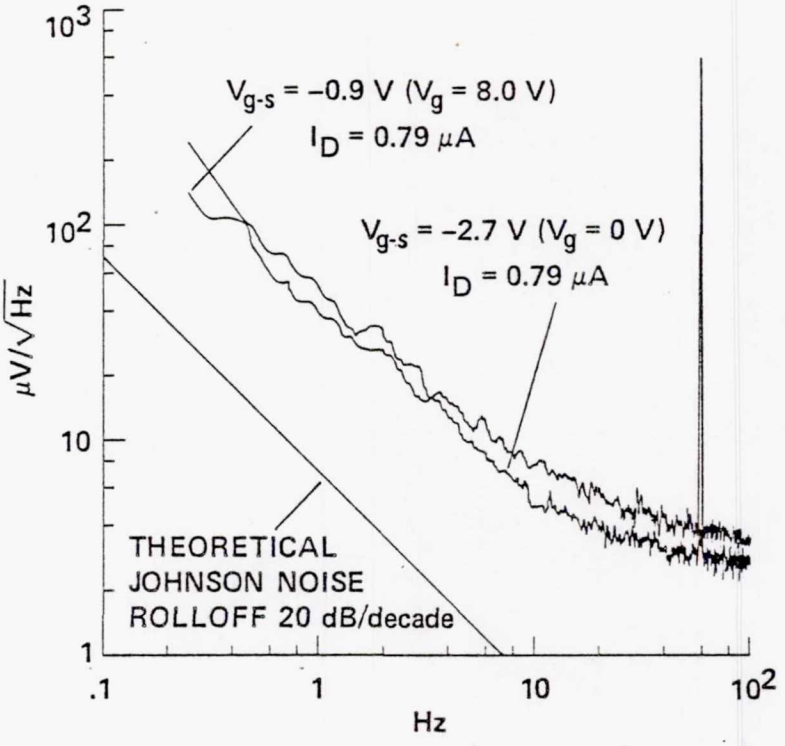


Figure 27.- CMOS MUX noise (static) — Channel 22: room temperature, BW_{amp} = 10 kHz.

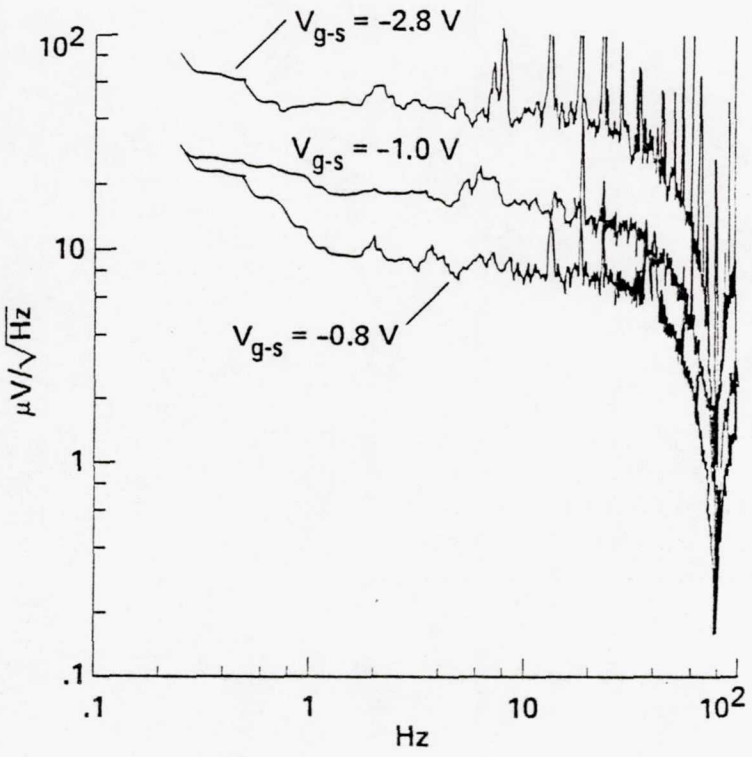


Figure 28.- CMOS MUX noise (clock rate = 3.2 kHz) — Channel 21: room temperature, I_{DS} = 0.14 μA, BW_{amp} = 19.4 kHz.

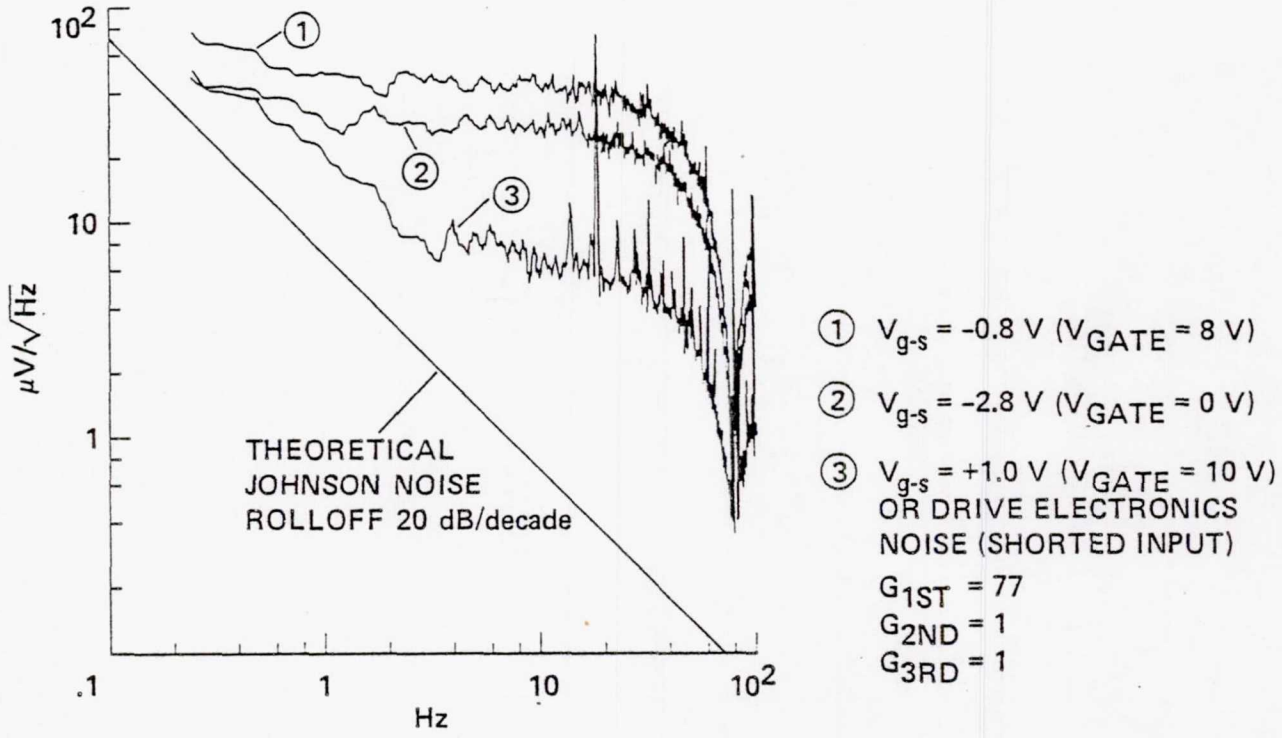


Figure 29.- CMOS MUX noise (clock rate = 3.2 kHz) — Channel 22: room temperature, I_{DS} = 0.7 μA, BW_{amp} = 19.4 kHz.

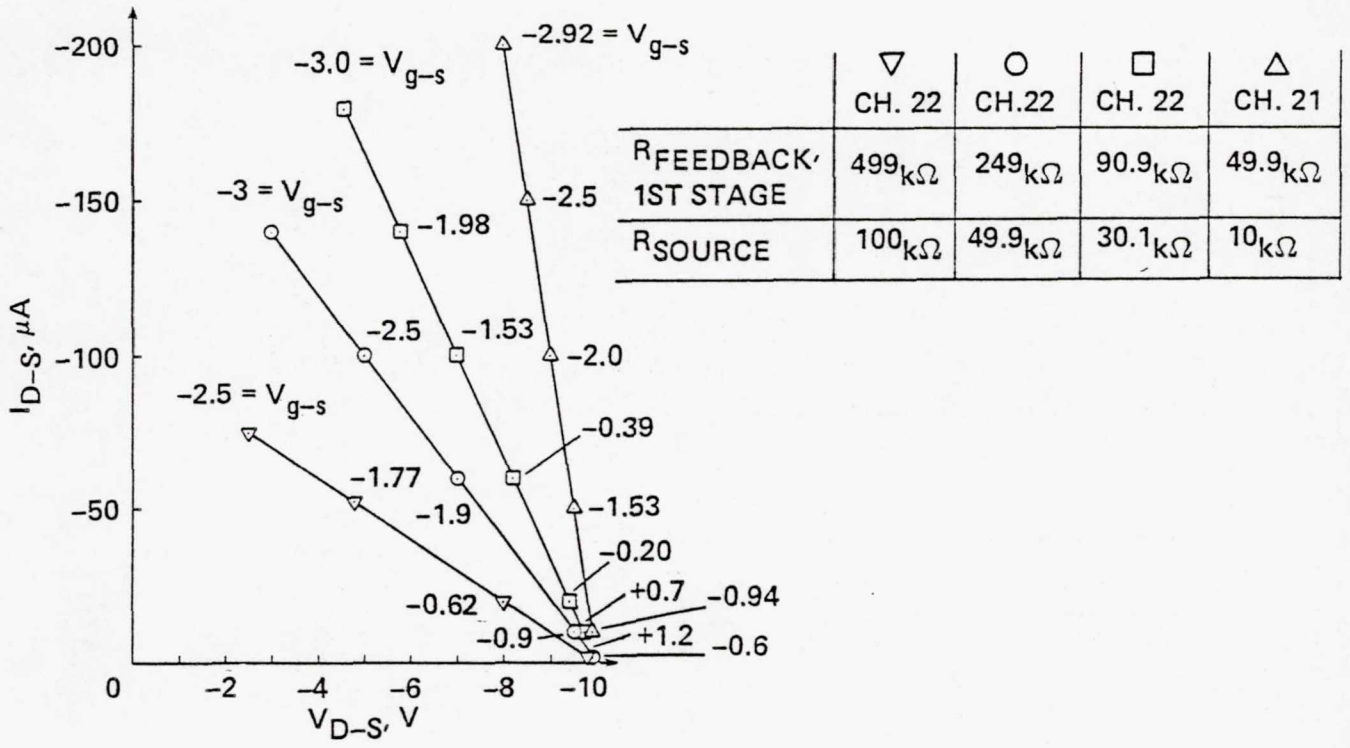


Figure 30.- CMOS MUX input FET drain current — voltage (drain-to-source) characteristics: at various source and first-stage feedback resistances.

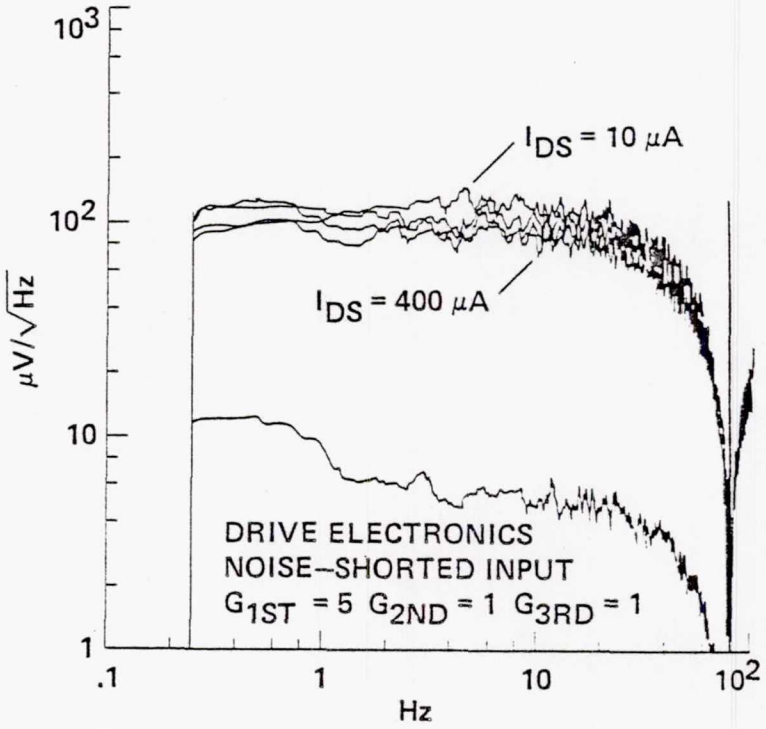


Figure 31.- CMOS MUX noise (clock rate = 3.2 kHz) — Channel 21: room temperature, BW_{amp} = 17.7 kHz.

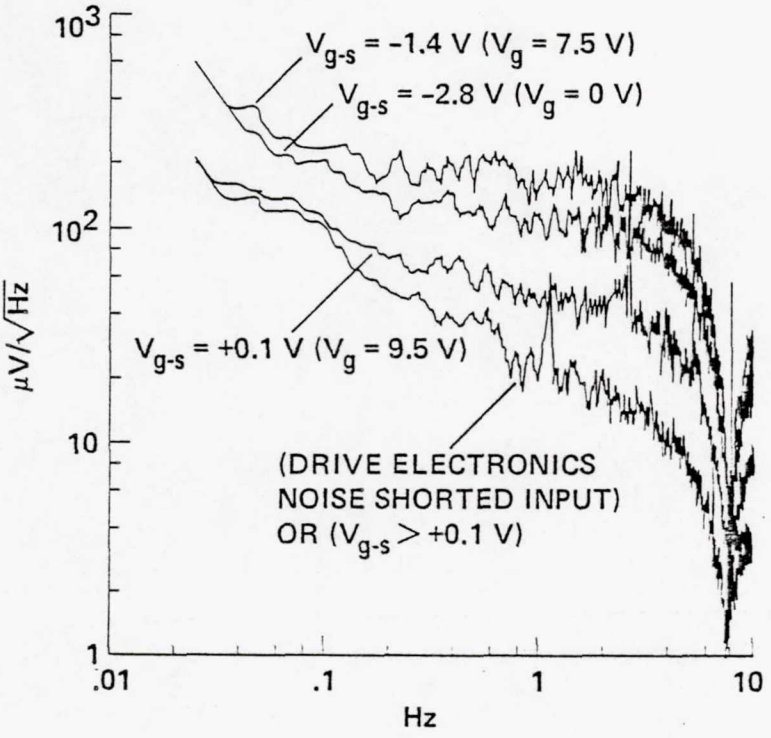


Figure 32.- CMOS MUX noise (clock rate = 320 Hz) — Channel 21: room temperature, BW_{amp} = 19.4 kHz.

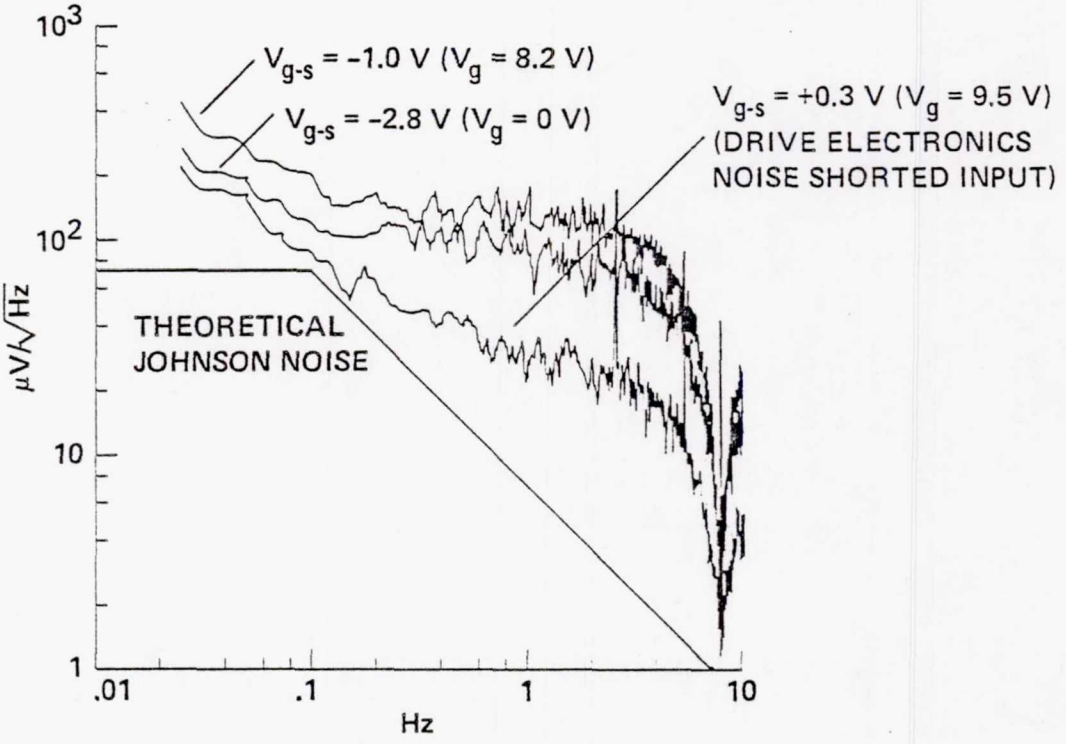


Figure 33.- CMOS MUX noise (clock rate = 320 Hz) — Channel 22: room temperature, BW_{amp} = 19.4 kHz.

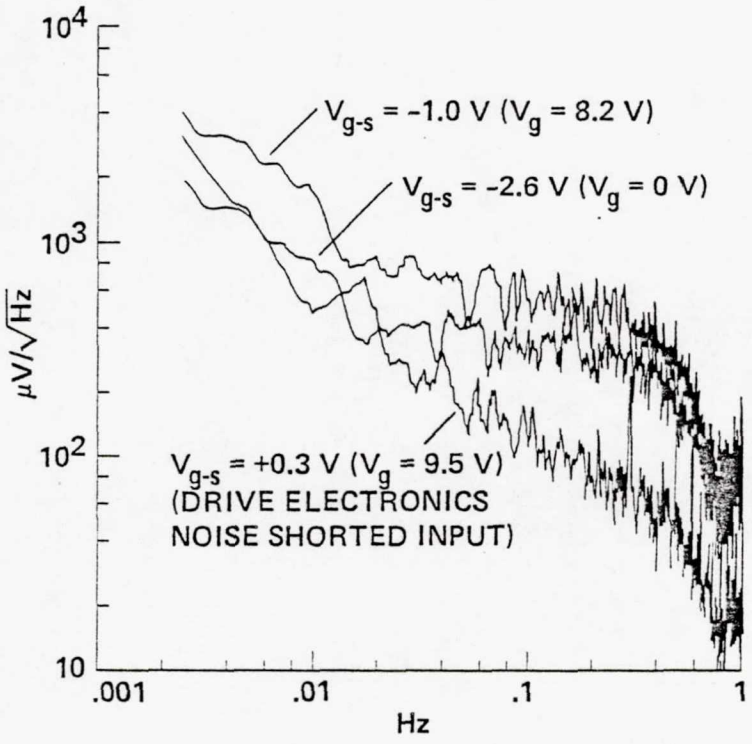


Figure 34.- CMOS MUX noise (clock rate = 32 Hz) — Channel 21: room temperature, BW_{amp} = 19.4 kHz.

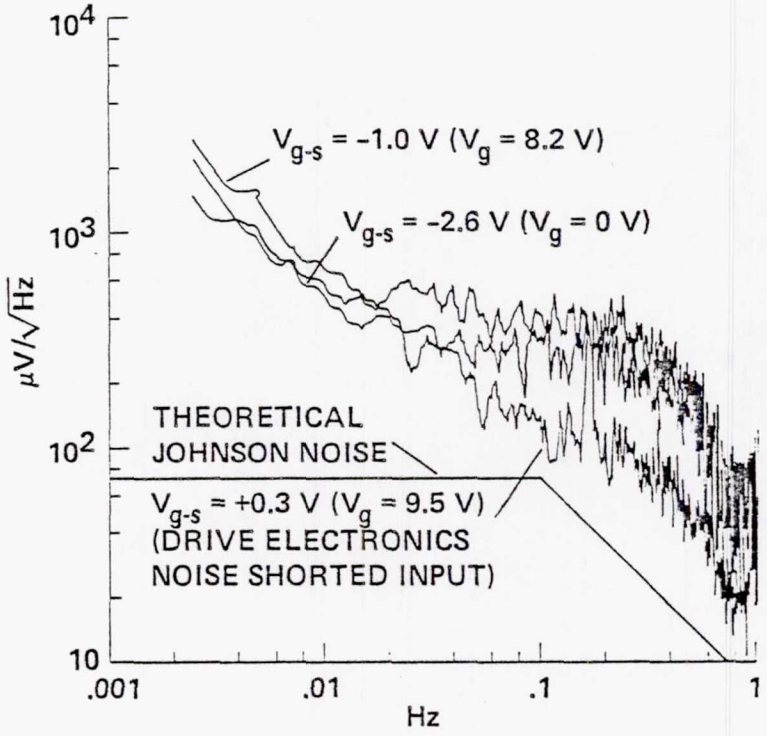


Figure 35.- CMOS MUX noise (clock rate = 32 Hz) — Channel 22: room temperature, BW_{amp} = 19.4 kHz.

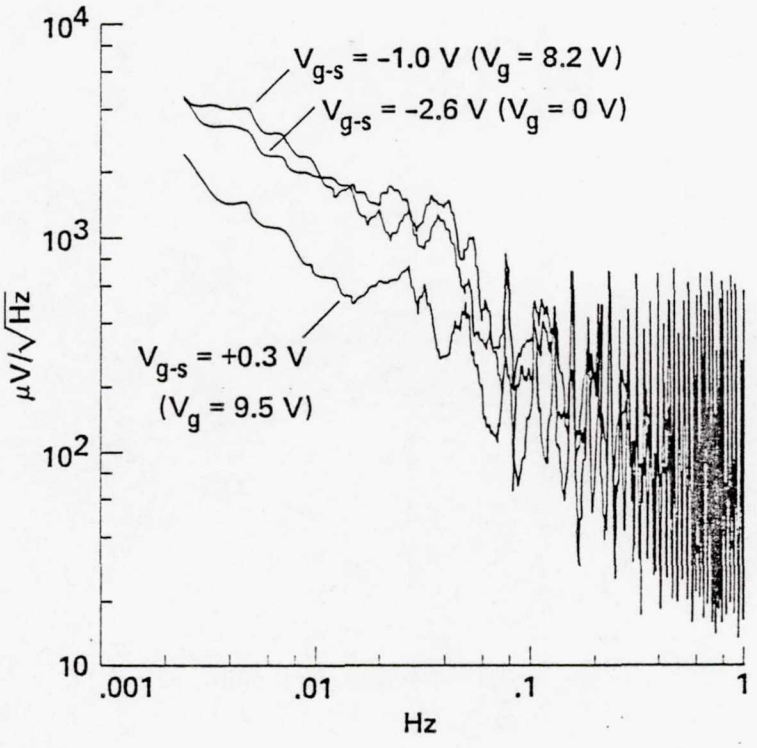


Figure 36.- CMOS MUX noise (clock rate = 3.2 Hz) — Channel 21: room temperature, BW_{amp} = 19.4 kHz.

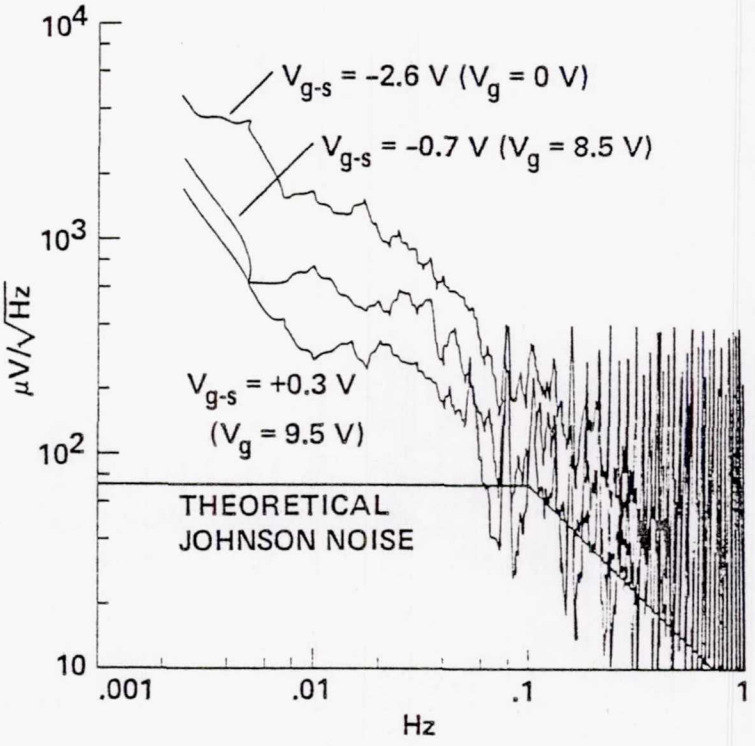


Figure 37.- CMOS MUX noise (clock rate = 3.2 Hz) — Channel 22: room temperature, BW_{amp} = 19.4 kHz.

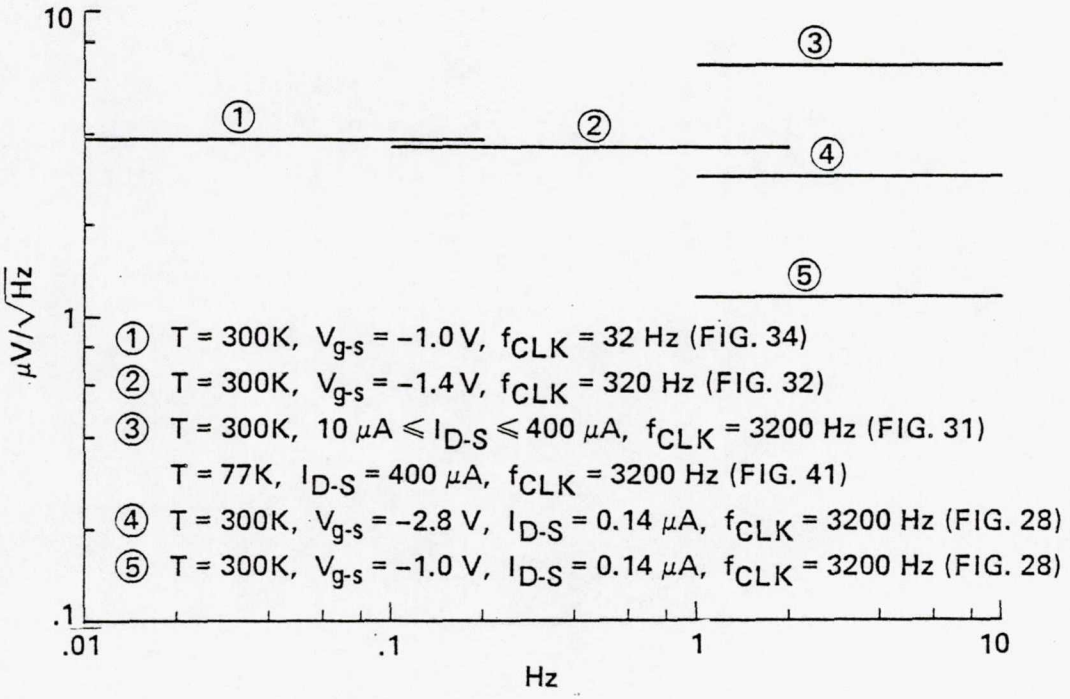


Figure 38.- "Bandwidth-corrected" CMOS multiplexer white noise: Channel 21 (with detector); dynamic mode.

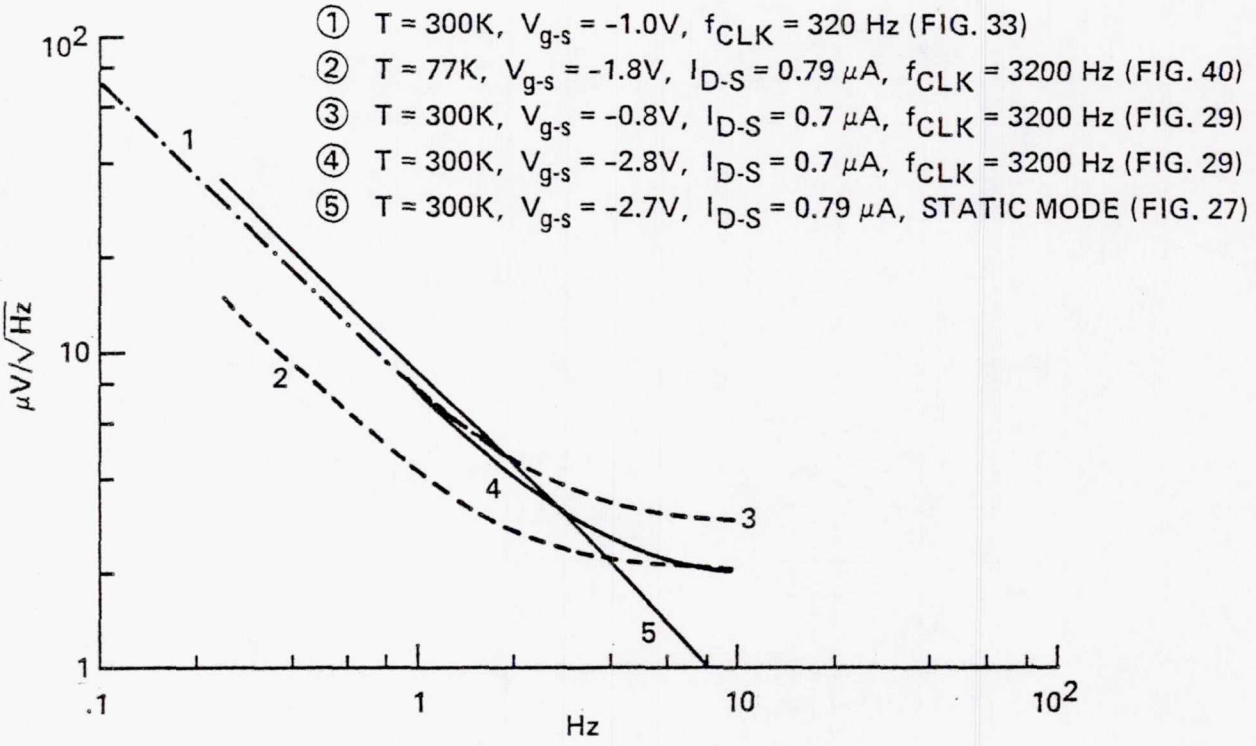


Figure 39.- "Bandwidth-corrected" CMOS multiplexer white noise and Johnson noise: Channel 22 (no detector).

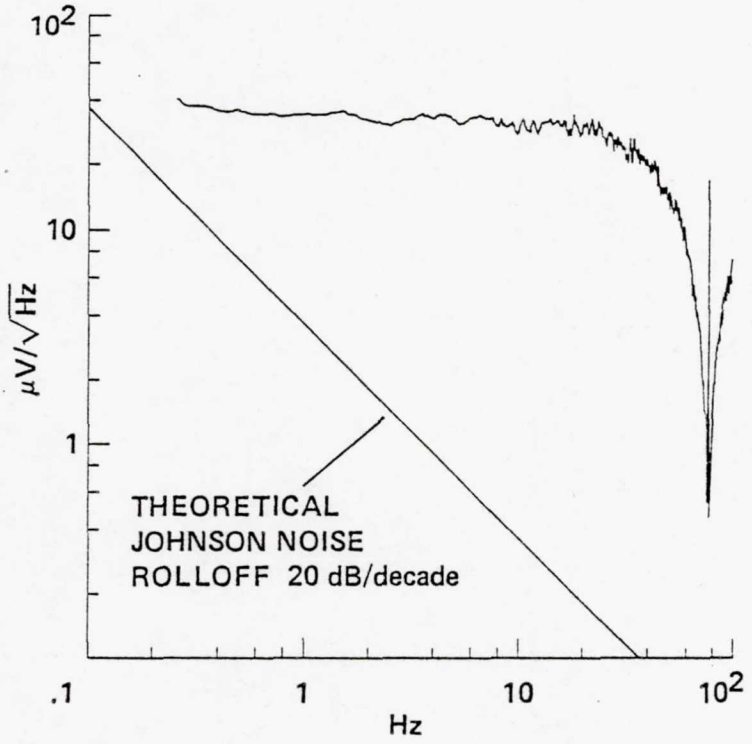


Figure 40.- CMOS MUX noise (clock rate = 3.2 kHz) — Channel 22: T = 77 K, I_{DS} = 0.79 μA, V_{gs} = -1.8 V, BW_{amp} = 19.4 kHz.

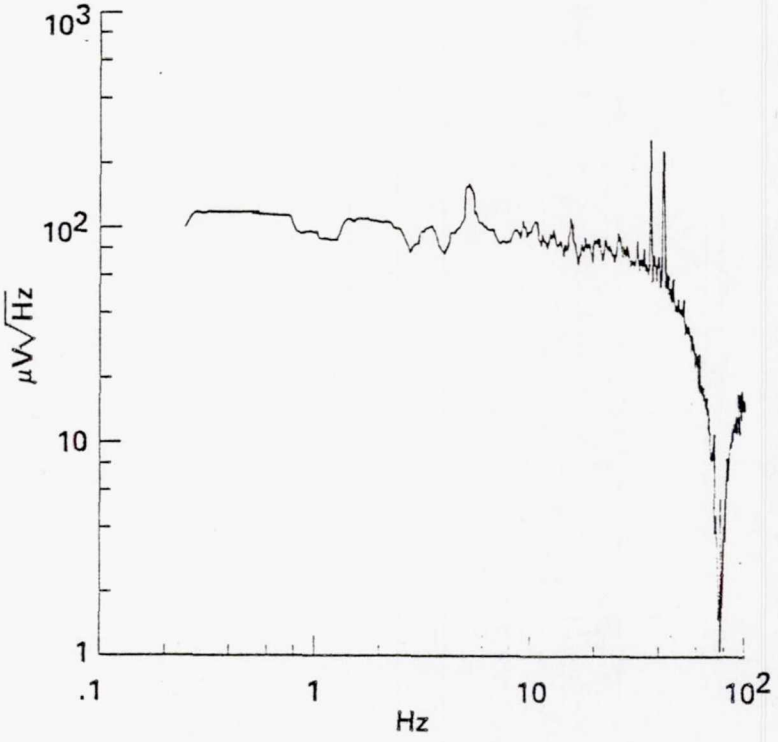


Figure 41.- CMOS MUX noise (clock rate = 3.2 kHz) — Channel 21: T = 77 K, I_{DS} = 400 μA, BW_{amp} = 17.7 kHz.

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15. Supplementary Notes

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16. Abstract

A 32-channel CMOS multiplexer was tested at room temperature and at liquid-helium temperature (4.9 K). Voltage gain of the FET input stage, leakage current, electrical crosstalk, and noise as a function of clock frequency were measured. The voltage gain measured at 4.9 K was slightly higher than that measured at 300 K and was independent of clock frequency at both operating temperatures. The off-channel leakage current was 0.23 pA/channel at 4.9 K. Electrical crosstalk between adjacent channels (one on, one off) was quite low. The spot noise at 10 Hz (7 $\mu V/\sqrt{Hz}$), of the CMOS multiplexer operating in the static mode did not vary significantly with operating temperature. In the dynamic mode (3.2-kHz clock) at room temperature, the spot noise at 10 Hz was substantially higher than that measured in the static mode.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
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